(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 874 471 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
28.10.1998 Bulletin 1998/44

(51) Int. Cl.[6]: **H04B 1/707**

(21) Application number: **98106931.3**

(22) Date of filing: **16.04.1998**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **24.04.1997 JP 107821/97**

(71) Applicant:
SHARP KABUSHIKI KAISHA
Osaka (JP)

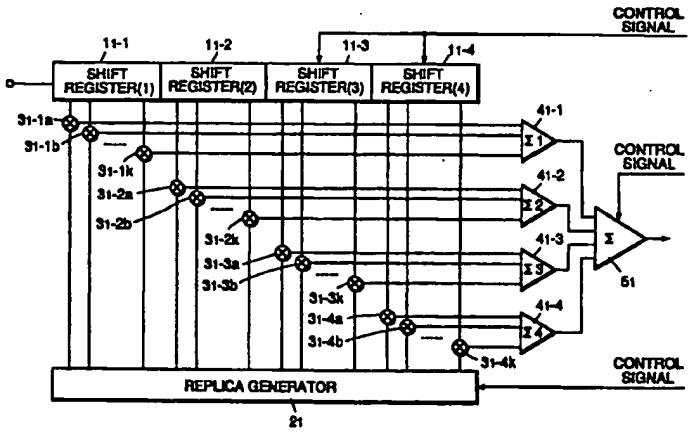
(72) Inventor: **Okamoto, Naoki**
Chiba-shi, Chiba (JP)

(74) Representative:
Müller, Frithjof E., Dipl.-Ing.
Patentanwälte
MÜLLER & HOFFMANN,
Innere Wiener Strasse 17
81667 München (DE)

(54) Direct sequence spread spectrum correlator

(57) The present invention is directed to reduce the lowering of transmission error and power consumption which is increased with the increase in the number of samples for enhancing the characteristics and to improve the characteristics. There are serially provided 4k (k denotes a spreading factor) shift registers (1) to (4) to deal with at most four samples to develop input spread signals, which are multiplied by spread-code replica signals from a replica generator (2_1). Sums Σ 1 to Σ 4 of respective k products are obtained. An output of a correlator is obtained by further adding the sums. At this time, the shift registers (1) to (4), adders (4_1-1 to 4) and the replica generator (2_1) are controlled in response to a control signal depending upon the number of samples. When three samples are sampled for one chip, the shift register (4) is disabled and (1, 1, 1, -1, -1, -1, 1, 1, 1, 1, 1, 1, -1, -1, -1, NA, NA, NA, NA, NA) are prepared as a replica and only adder Σ 4 is disabled and an output of the correlator is obtained from signals stored in the shift registers (1), (2), (3).

FIG.7



EP 0 874 471 A2

Description

BACKGROUND OF THE INVENITON

The present invention relates to a wireless or wire communication and in particular to a spread spectrum communication system using direct spreading and a demodulator used in the spread spectrum communication system according to sampling received signals, which may be widely used for digital data communication.

Various modulation systems have conventionally used for wireless data communications. Among of them, the spread spectrum communication system has attracted attention as a new communication system.

The modulation systems which are commonly used for data communication are narrow-band width modulation system and can be implemented by a relatively small circuit, but has a drawback that it is sensitive to the multi-path or narrow-band non-white noise indoors (in offices or factories and the like).

In contrast to this, the spread spectrum communication system is advantageous in that these drawbacks can be overcome since the transmission spectrum of signals for carrying data is spread in accordance with a spread-code (code used for spreading) so that the signals are transmitted at a broad-band width.

Among of the spread spectrum transmitting systems, the direct spread (DS) system has been put into practice in some areas.

Now, an exemplary configuration of transmission and reception sides of a communication device used for the DS communication system, respectively will be described.

This example is designated as a communication device for demodulating the signals which has been modulated by BPSK modulation technique and transmitted.

On the transmission side, data to be transmitted from a data generating unit is spread in a spreading unit by using spreading codes which are generated by a spread-code generating unit. The data is spread by a factor of k wherein k denotes the length of the spread-code. The data which was spread will be referred to as "spread data". The unit of data to be transmitted is referred to as "one bit" and the unit of spread data is referred to as "one chip". In other words, one bit comprises k chips. Thereafter, the spread signal modulates an oscillation signal from a RF oscillator in a modulating unit and is transmitted from an antenna via a radio frequency circuit (not shown).

On the other hand, the transmitted signal is received by an antenna and is fed to a radio frequency circuit for converting it into an IF signal.

In the receiver, the received IF signal is divided by a dividing-by-two splitter into two signals which are input to multipliers, in which two signals are converted into I and Q components of a base band by using cosine and sine components of a local signal from a local signal oscillator (VCO).

Conversion into I and Q components is carried out by using sine and cosine components from the local signal oscillator. Alternatively, it may be done by using a signal line and a phase-shifter for shifting one of the components of the local signal by 90 degrees.

The I and Q components of the base band are then sampled for quantization by A/D convertors, respectively so that they are converted into digital data. The data are input into digital correlators for establishing correlations concerning to the respective data. The respective correlation outputs are fed to a timing detector and latch circuits. The timing detector detects correlation spikes and causes respective correlation outputs to be latched in a timed relationship with the detected correlation spikes so that they can be demodulated to provide data.

In the receiver having such a configuration, sampling of plural samples such as two or three samples per one chip is conducted independently of the data or chip. This is due to the fact that C/N ratio prior to despreading is very low and it is hard to conduct regeneration of clock before despreading in the spread spectrum communication.

The correlators establish a correlation relationship by using all values of samples.

Accordingly, a correlation is determined in the digital correlator by using values of 2k samples when two samples to one chip.

The manner of sampling in the base band in this case is refered to an eye pattern based on chip.

Inherently, the eye is most wide at the midpoint of the eye pattern and decreases its size as it becomes closer to the opposite ends thereof. The theoretical value of the error rate in the digital communication is generally a value which is measured at the midpoint of the eye pattern.

In an example in which two samples are sampled to one chip, a timing relationship is designated that the two samples are substantially equally sampled with respect to the eye pattern. Although the eye is slightly smaller in amplitude than that at the midpoint in this case, both samples are valid.

On the other hand, in the timing relationship of one sample is sampled at the midpoint of the eye pattern so the amplitude is larger. Since the other sample is sampled at a transition point of the chip, the value of the other sample is almost invalid.

Therefore, a problem occurs that the characteristics may be deteriorated depending upon the sampling timing relationship if two samples are sampled from one chip independently of the timing relationship with of the chip like prior art.

The inventors of the present application have proposed a communication system in which data are serial/parallel-converted and spread in accordance with the same spreading code and multiplexed for communi-

cation.

In this system, spread signals are delayed and multiplexed for high rate transmission in a limited band. This system will be referred to as "delayed multiplexing technique".

This system enables high rate transmission to be conducted in a limited band. Communication of data at 4 and 10 MBPS is possible when two and five signals are multiplexed, respectively.

In an exemplary configuration of a transmitting system for delayed multiplexing technique, the data which is generated in a data generating unit are coded as differential-valued data by a differential coding unit and then converted into a number of parallel signals, the number of which is equal to the number of signals to be multiplexed by an S/P converting unit. The converted parallel signals are multiplied by a PN code from a PN generator in multipliers for spreading.

Subsequently, the spread signals are delayed by delay elements, respectively and are mixed by a mixer to provide a multi-valued digital signal, which modulates an oscillation signal from an RF oscillator in a modulator. The modulated signal is frequency-converted by a frequency converting unit and is transmitted via a power amplifying unit, etc.

High rate data communication is made possible by receiving and demodulating the signals which are multiplexed on the transmitting side of the communication system which has conducted delayed multiplexing in such a manner.

Since the signals to be transmitted are multi-valued signals as shown in an eye pattern in the delayed multiplexing system, the error would become larger if the samples are sampled at the transition points of the data.

If the normalized value of the eye pattern is assumed to be 1, the value of the eye pattern only changes in the range of 1 to -1 when multiplexing is conducted, the eye pattern only would change 1 to 0 at the transition position of the data. If multiplexing is conducted, the value of the eye pattern would change in the range of 1 to 5. In this case, the value at the transition position would change 1 to 3, causing substantial deterioration.

In order to avoid this deterioration, increasing the number of samples may be envisaged.

This may be applied to the multiplexing configuration as well as general CDMA communication in which multiplexing is conducted by spreading signals with different codes.

If there is one sample at the transition position of data when three samples are sampled to one chip, one second of samples would be valid while when three samples are sampled to one chip, two thirds of samples would be valid. An improvement in characteristics can be correspondingly expected. If four samples are sampled to one chip, three fourths of samples would be valid, an improvement in characteristics can be expected.

However, another problem may occur that the power consumption will be increased due to an increased number of samples.

A prior art correlator relying upon a plurality of samples comprises shift registers; a replica-generating unit having a spreading code data; a number of multipliers the number of which is equal to the number of samples and an adder for adding the outputs from the multipliers. The correlator has on its input side shift registers, the number of which is equal to the number of samples for holding data of an input signal. Since the shift registers require the circuits, the number of which is equal to the number of input signals for each of samples (for example, three and four circuits when one sample comprises three and four bits, respectively), its power consumption is high. Since most of circuits comprise shift registers in the correlator, the power consumption for two samples is substantially double as much as that for four samples.

SUMMARY OF THE INVENTION

The present invention was made in view of the above-mentioned problems in the prior art of the direct spread spectrum communication system. It is an object of the present invention to achieve an improvement in characteristics by minimizing the power consumption which is increased as the number of samples is increased in a technique for sampling a plurality of samples, which is capable of decreasing the transmission error and improving the characteristics.

(1) One of the present invention resides in a demodulating device in the direct spread spectrum communication system having sampling means for sampling a given number of samples to one chip from input spread signals in a base band area, which are directly spread with a spread-code, said demodulating device being adapted to perform despreading based upon discrete sample signals which are obtained by said sampling means for demodulation, in which said sampling means in which the number of samples can be controlled in response to a control signals is used.

(2) Another one of the present invention resides in a correlator in the direct spread spectrum communication system having sampling means for sampling a given number of samples to one chip from input spread signals in a base band area, which are directly spread with a spread code, the correlator being adapted to determine a correlation between discrete sample signals by multiplying discrete sample signals which are obtained by said sampling means by a reference spread signal prepared relevant to one code-length of said spread-signal for said discrete sample signals and by adding the results of multiplication in each chip when demodulation is performed by conducting despreading based upon said discrete sample signals, in which

said correlator comprises a number of in-series-connected shift registers being inputted said discrete sample signals, the number of which is equal to the maximum number of samples to one chip and replica signal generating means for generating a number of replica signals, the number of which is equal to the number of samples per the same chip as replica of said reference spreading signal.

(3) Another one of the present invention resides in a correlator in the direct spread spectrum communication system having sampling means for sampling a given number of samples per one chip from input spread signals in a base band area, which are directly spread with a spread code, the correlator being adapted to determine a correlation between discrete sample signals by multiplying discrete signals which are obtained by said sampling means by a reference spreading signal prepared relevant to one code-length of said spread-code for said discrete sample signals and by adding the results of multiplication in each chip when demodulation is performed by conducting despreading based upon said discrete sample signals, in which said correlator comprises a number of in-parallel-connected shift registers being inputted said discrete sample signals, the number of which is equal to the maximum number of samples to one chip and replica signal generating means for generating a number of replica signals, the number of which is equal to the number of samples per the same chip as replica of said reference spreading signal.

(4) Another one of the present invention resides in a demodulating device in the direct spread spectrum communication system as mentioned of (1) above, in which a control signal is generated for controlling said number of samples depending upon the multi-valued number which the signal level of said input spread signals has.

(5) Another one of the present invention resides in a demodulating device in the direct spread spectrum communication system as mentioned of (1) above, in which when a signal in a predetermined data format including a non-multiplexed portion containing data for defining the communication format, etc., which is followed by a multiplexed portion is input as said input spread signals, a control signal for controlling the number of samples, which is preset in said non-multiplexed portion, or a control signal for controlling the number of samples depending upon the multi-valued number which the signal level of multiplexed spread signal has in the multiplexed portion is generated as a control signal for controlling said number of samples.

(6) Another one of the present invention resides in a demodulating device in the direct spread spectrum communication system as mentioned of (4) above, in which when a signal in a predetermined data format including a non-multiplexed portion containing data for defining the communication format, etc., which is followed by a multiplexed portion is input as said input spread signals, a control signal for controlling the number of samples is generated by using a multi-valued number which is obtained by identifying the multi-valued number which has been incorporated in said non-multiplexed portion.

(7) Another one of the present invention resides in a demodulating device in the direct spread spectrum communication system having means for sampling a given number of samples to one chip from input spread signals in a base band area, which are directly spread with a spread-code, said demodulating device being adapted to perform despreading based upon discrete sample signals which are obtained by said sampling means for demodulation, in which said demodulating device comprises sample signal selecting means for selecting a number of samples, the number of which is less than a given number of samples of each chip from the discrete sample signals which are obtained by sampling of said sampling means to despread only sample signals which are selected by said sample signal selecting means for demodulation.

(8) Another one of the present invention resides in a demodulator device in the direct spread spectrum communication system as mentioned of (7) above, in which said sample signal selecting means selects sample signals in such a timing relationship that a correlation signal is generated, which is detected in a clock regenerating circuit for regenerating sampling clock signals based upon despread signals which are obtained by adding correlation signals based on all sample signals which are sampled by said sampling means.

(9) Another one of the present invention resides n a demodulating device in the direct spread spectrum communication system as mentioned of (8) above, in which said despread signals which are obtained by adding correlation signals based on said all sample signals are obtained by adding signals which are obtained by despreading sample by sample a given number of sample signals of each chip, which are obtained by said sampling means.

(10) Another one of the present invention resides in a demodulator device in the direct spread spectrum communication system as mentioned of (8) or (9) above, in which when despreading is performed by sampling an even number of samples to one chip and by using a passive type of correlator, a sample signal is selected which corresponds to larger one of previous and subsequent correlation MAG outputs with respect to the midpoint of a timing interval in which correlation signals which are detected by said clock regenerating circuit are generated.

(11) Another one of the present invention resides in a demodulator device in the direct spread spectrum

communication system as mentioned of (8) or (9) above, in which when despreading is performed by sampling an odd number of samples to one chip and by using a passive type of correlator, discrete sample signals are selected in a clock timing relationship in which correlation signals which are detected by said clock regenerating circuit are generated.

(12) Another one of the present invention resides in a demodulating device in the direct spread spectrum communication as mentioned of any one of (8) to (11) above, in which said clock regenerating circuit comprises correlation signal integrating means for detecting the timing relationship in which correlation signal are generated and integrating means for selecting sample signals, which is separate from said integrating means for clock generating.

(13) Another one of the present invention resides in a demodulating device in the direct spread spectrum communication system as mentioned of (12) above, in which the number of integration operations depending upon the discrete sample signals which are performed in said integrating means for selecting sample signals is determined and preset as a function of data rate and spreading rate, based upon the accuracy of an oscillator used in said communication system.

(14) Another one of the present invention resides in a demodulating device in the direct spread spectrum communication system as mentioned of any one of (7) to (13) above, in which when signals which have been spread by using the same spread-code, delayed and multiplexed are input as said input spread signals, the sample signals which are selected depending upon the operation of said sample signals are changed each block unit of said delayed and multiplexed signals so that the condition of selecting of the sample signals is maintained for a period of said block unit.

(15) Another one of the present invention resides in a demodulating device in the direct spread spectrum communication system in which the sampling means of the demodulator device in the direct spread spectrum communication system as mentioned of any one of (1), (4), (5) and (6) above is used as sampling means of the demodulating device in the direct spread spectrum communication system as mentioned of any one of (7) to (14) above.

In accordance with the present invention, the number of samples can be preset in view of power consumption and characteristics by means for changing the number of samples in response to a control signal.

Further, in accordance with the present invention, a number of shift registers, the number which is equal to the maximum number of samples are in series connected to each other and corresponding number of replicas are generated. The number of samples is changed in response to an externally provided control signal.

If the transmitted signals have multi-valued signal levels to which several spread signals are added, optimal characteristics could be obtained for each multi-valued number by changing the number of samples to be controlled depending upon the multi-valued number.

In a system for transmitting plural series of signals which are multiplexed by delaying desired several chips by desired several chips signals which are spread with the same spreading code as that of a non-multiplexed portion in a data format, optimum characteristics can be obtained over both non-multiplexed portion and multiplexed portion by changing the number of samples between non-multiplexed and multiplexed portions. Alternatively, signals carrying the number of signals to be multiplexed may be transmitted and the number of signals to be multiplexed is identified on the receiving side. The number of samples can be switched from the multiplexed portion depending upon the identified number of signals to be multiplexed.

Demodulation can be performed only in an region having a better C/N ratio by using one sample or m samples per chip of signals which are sampled by sampling several samples (k samples) (k>m) per one chip.

Using a clock regenerating circuit for regenerating clock by using despread signals which are obtained by adding all samples makes it possible to select much better region having a much better C/N ratio.

In the foregoing invention, a circuit can be commonly used by obtaining the despread signals by adding signals which are despread one sample by one sample.

If an even number of samples (for example, two samples per one chip) are sampled, a larger MAG output is selected from previous and subsequent samples with respect to the midpoint of an eye pattern. A sample which is in a region having a better C/N ratio of an eye pattern can be positively selected by selecting previous or subsequent sample if the previous sample is larger than the subsequent sample or vice versa.

If an odd number of samples (for example, three samples per one chip) are sampled, a region of an eye pattern having a better S/N ratio can be positively selected by performing sampling in the timing relationship of clock regeneration.

The integration for selection can be switched more rapidly by being replaced with the integration for clock regeneration.

The number of integration operations can be switched depending upon the system with reference to the accuracy of the oscillator used for the communication system, data rate and spreading rate.

Cancellation of cross interference can be performed in an excellent manner by selecting each unit of multiplexed block in a system in which transmitted and received signals are multiplexed.

A system having a low power consumption and

excellent characteristics can be built by combining a method of selecting signals used for demodulation from sampled signals with the method of selecting the number of samples.

BRIEF DESCRIPTION OF THE DRAWINGS

[Fig. 1] A block diagram for explaining the configuration of the general spread spectrum communication system on the transmitter side.

[Fig. 2] A block diagram for explaining the configuration of the general spread spectrum communication system on the receiver side.

[Fig. 3] Time charts showing the timing relationship between the eye pattern of the base band signal and sampled signals.

[Fig. 4] A block diagram showing an example of the prior art circuit configuration of a system for delaying and multiplexing by spreading with the same code in the direct spread spectrum communication.

[Fig. 5] Time charts showing eye patterns of multiplexed base band signals in Fig. 4.

[Fig. 6] A circuit block diagram showing an example of the configuration of a prior art correlator using a plurality of samples.

[Fig. 7] A circuit block diagram showing the configuration of an embodiment of a correlator of the present invention.

[Fig. 8] A circuit block diagram showing the configuration of an embodiment of another correlator of the present invention.

[Fig. 9] A circuit block diagram showing an example of the configuration adapted to the multiplexing system of the present invention.

[Fig. 10] A view showing a data format having a non-multiplexed portion and multiplexed portion which is processed in a system using a demodulating device of the present invention.

[Fig. 11] A circuit block diagram showing the configuration of a further correlator of the present invention.

[Fig. 12] A circuit block diagram showing the configuration of a clock regenerating circuit which is used for selecting sampling clock signal in correlation processing in accordance with the present invention.

[Fig. 13] A circuit block diagram showing in detail a clock generator which is a component of the clock regenerating circuit in Fig. 12.

[Fig. 14] A circuit block diagram showing the configuration of a circuit for carrying out a method of selecting sampling clock signals in correlation processing in accordance with the present invention.

[Fig. 15] Time charts showing an eye pattern of base band signals, sample signals, clock regeneration and MGA outputs in operation of the correlator of the present invention.

[Fig. 16] Time charts showing another condition of an eye pattern of base band signals, sample signals, clock regeneration and MGA outputs in operation of the correlator of the present invention.

[Fig. 17] Time charts showing a further condition of an eye pattern of base band signals, sample signals, clock regeneration and MGA outputs in operation of the correlator of the present invention.

[Fig. 18] A circuit block diagram showing the configuration of an embodiment of a further correlator of the present invention.

[Fig. 19] A circuit block diagram showing the configuration of an embodiment of a further correlator of the present invention.

[Fig. 20] A circuit block diagram showing the configuration of the clock regenerating circuit of the present invention used for selecting sample signals, which is added with another adders.

[Fig. 21] Time charts showing the amplitude of eye patterns at two sampling times for explaining the operation of the present invention.

[Fig. 22] A circuit block diagram showing an example of the configuration of an embodiment of the demodulating device of the present invention.

PREFERRED EMBODIMENTS OF THE INVENTION

The present invention relates to a wireless or wire communication and in particular to a spread spectrum communication system using direct spreading and a demodulator used in the spread spectrum communication system according to sampling received signals, which may be widely used for digital data communication.

Prior to explaining preferred embodiments of the present invention, prior art demodulating device in direct spread spectrum communication system and prior art correlator in the same system will be described below as references for the present invention.

Various modulation systems have conventionally used for wireless data communications. Among of them, the spread spectrum communication system has attracted attention as a new communication system.

The modulation systems which are commonly used for data communication are narrow-band width modulation system and can be implemented by a relatively small circuit, but has a drawback that it is sensitive to the multi-path or narrow-band non-white noise indoors (in offices or factories and the like).

In contrast to this, the spread spectrum communication system is advantageous in that these drawbacks can be overcome since the transmission spectrum of signals for carrying data is spread in accordance with a spread-code (code used for spreading) so that the signals are transmitted at a broad-band width.

Among of the spread spectrum transmitting systems, the direct spread (DS) system has been put into practice in some areas.

Now, the configuration of the direct spread spectrum communication system will be described with reference to attached drawings.

Figs. 1 and 2 show an exemplary configuration and are block diagrams illustrating the transmission and reception sides of a communication device used for the DS communication system, respectively.

This example shows a communication device for demodulating the signals which has been modulated by BPSK modulation technique and transmitted.

On the transmission side, data to be transmitted from a data generating unit 101 is spread in a spreading unit 102 by using spreading codes which are generated by a spread-code generating unit 102c. The data is spread by a factor of k wherein k denotes the length of the spread-code. The data which was spread will be referred to as "spread data". The unit of data to be transmitted is referred to as "one bit" and the unit of spread data is referred to as "one chip". In other words, one bit comprises k chips. Thereafter, the spread signal modulates an oscillation signal from a RF oscillator 103s in a modulating unit 103 and is transmitted from an antenna via a radio frequency circuit (not shown).

On the other hand, the transmitted signal is received by an antenna and is fed to a radio frequency circuit for converting it into an IF signal.

In the receiver, the received IF signal is divided by a dividing-by-two splitter 104 into two signals which are input to multipliers 105 and 106, in which two signals are converted into I and Q components of a base band by using cosine and sine components of a local signal from a local signal oscillator (VCO) 107.

Conversion into I and Q components is carried out by using sine and cosine components from the local signal oscillator 107. Alternatively, it may be done by using a signal line and a phase-shifter for shifting one of the components of the local signal by 90 degrees.

The I and Q components of the base band are then sampled for quantization by A/D convertors 108 and 109, respectively so that they are converted into digital data. The data are input into digital correlators 110 and 111 for establishing correlations concerning to the respective data. The respective correlation outputs are fed to a timing detector 112 and latch circuits 113 and 114. The timing detector detects correlation spikes and causes respective correlation outputs to be latched in a timed relationship with the detected correlation spikes so that they can be demodulated to provide data.

In the receiver having such a configuration, sampling of plural samples such as two or three samples per one chip is conducted independently of the data and/or chip. This is due to the fact that C/N ratio prior to despreading is very low and it is hard to conduct regeneration of clock before despreading in the spread spectrum communication.

The correlators establish a correlation relationship by using all values of samples.

Accordingly, a correlation is determined in the digital correlator by using values of 2k samples when two samples to one chip.

The manner of sampling in the base band in this case is illustrated in Fig. 3 with reference to an eye pattern based on chip.

Inherently, the eye is most wide at the midpoint of the eye pattern and decreases its size as it becomes closer to the opposite ends thereof. The theoretical value of the error rate in the digital communication is generally a value which is measured at the midpoint of the eye pattern (refer to Fig. 3).

An example in which two samples are sampled to one chip is shown in Fig. 3.

A timing relationship A of Fig. 3 shows that the two samples (a) and (b) are substantially equally sampled with respect to the eye pattern. Although the eye is slightly smaller in amplitude than that at the midpoint in this case, both samples are valid.

On the other hand, in the timing relationship B of Fig. 3, the sample (c) is sampled at the midpoint of the eye pattern so the amplitude is larger. Since the other sample (d) is sampled at a transition point of the chip, the value of the other sample (d) is almost invalid.

Therefore, a problem occurs that the characteristics may be deteriorated depending upon the sampling timing relationship if two samples are sampled from one chip independently of the timing relationship with of the chip like prior art.

The inventors of the present application have proposed a communication system in which data are serial/parallel-converted and spread in accordance with the same spreading code and multiplexed for communication.

In this system, spread signals are delayed and multiplexed for high rate transmission in a limited band. This system will be referred to as "delayed multiplexing technique".

This system enables high rate transmission to be conducted in a limited band. Communication of data at 4 and 10 MBPS is possible when two and five signals are multiplexed, respectively.

An exemplary configuration of a transmitting system for delayed multiplexing technique is shown in Fig. 4.

Now, the configuration will be described with reference to Fig. 4. The data which is generated in a data generating unit 121 are coded as differential-valued data by a differential coding unit 122 and then converted into a number of parallel signals, the number of which is equal to the number of signals to be multiplexed by an S/P converting unit 123. The converted parallel signals are multiplied by a PN code from a PN generator 125 in multipliers 124-1 through 124-5 for spreading.

Subsequently, the spread signals are delayed by delay elements 126-1 through 126-5, respectively and are mixed by a mixer 127 to provide a multi-valued digital signal, which modulates an oscillation signal from an RF oscillator 129 in a modulator 128. The modulated signal is frequency-converted by a frequency converting unit 130 and is transmitted via a power amplifying unit 131, etc.

High rate data communication is made possible by receiving and demodulating the signals which are multiplexed on the transmitting side of the communication system which has conducted delayed multiplexing in such a manner.

An eye pattern in the delayed multiplexing system is shown in Fig. 5. Since the signals to be transmitted are multi-valued signals, the error would become larger if the samples are sampled at the transition points of the data.

If the normalized value of the eye pattern is assumed to be 1, the value of the eye pattern only changes in the range of 1 to -1 when multiplexing is conducted, the eye pattern only would change 1 to 0 at the transition position of the data. If multiplexing is conducted, the value of the eye pattern would change in the range of 1 to 5 as shown in Fig. 5. In this case, the value at the transition position would change 1 to 3, causing substantial deterioration.

In order to avoid this deterioration, increasing the number of samples may be envisaged.

This may be applied to the multiplexing configuration as shown in Fig. 4 as well as general CDMA communication in which multiplexing is conducted by spreading signals with different codes.

If there is one sample at the transition position of data when three samples are sampled to one chip, one second of samples would be valid while when three samples are sampled to one chip, two thirds of samples would be valid. An improvement in characteristics can be correspondingly expected. If four samples are sampled to one chip, three fourths of samples would be valid, an improvement in characteristics can be expected.

However, another problem may occur that the power consumption will be increased due to an increased number of samples.

The configuration of a prior art correlator relying upon a plurality of samples is illustrated in Fig. 6.

In Fig. 6, a reference numeral 116 denotes shift registers; 117 a replica-generating unit having a spreading code data; 118-1 to 118-n a number of multipliers the number of which is equal to the number of samples; 119 an adder for adding the outputs from the multipliers 118-1 to 118-n. The correlator has on its input side shift registers 116, the number of which is equal to the number of samples for holding data of an input signal. Since the shift registers 116 require the circuits, the number of which is equal to the number of input signals for each of samples (for example, three and four circuits when one sample comprises three and four bits, respectively), its power consumption is high. Since most of circuits comprise shift registers in the correlator, the power consumption for two samples is substantially double as much as that for four samples.

A first embodiment of the present invention will be described with reference to Fig. 7.

Fig. 7 shows the configuration of one embodied circuit of a correlator of the present invention.

Prior to description of the correlator of Fig. 7, the configuration of the circuit of the above-mentioned prior art correlator shown in Fig. 6 is described. In the prior art correlator, sampled incoming base band signals are successively stored in the shift registers 116.

If two samples are sampled to one chip, the number of the shift registers would be 2k (k represents the spreading factor). If the input signal is a multi-bit digital signal, the number of the shift registers would be multiplied by the number of bits.

The signal which is stored in each of shift registers is multiplied by a replica 117 in each of the multipliers 118-1 to 118-n. The replica 117 is a spread-code per se. If two samples are sampled to one chip, the signal is multiplied by the same code two times, as follows (1,2), (3,4), (5,6) ...so on.

Specifically, if the spread-code is (1, -1, 1, 1, - 1), the replica would be (1, 1, -1, -1, 1, 1, 1, 1, -1, -1).

On the other hand, the number of samples can be changed in response to a control signal in the embodiment of the present invention.

An example in which the number of samples can be selected among three numbers, such as 2, 3, 4 is shown in Fig. 7.

The sampled input signals are input to the shift registers (1) 1_1-1 to (4) 1_1-4. The length of the shifts registers (1) 1_1-1 to (4) 1_1-4 is a value which obtained by multiplying the length of the spread-code by the maximum number of samples to one chip.

In the drawing, 4k shift registers (1) 1_1-1 to (4) 1_1-4 are provided so that at most four samples will be sampled wherein k denotes the spreading factor (or the number of chips). The signal which is stored in each of the shift registers (1) 1_1-1 to (4) 1_1-4 is multiplied by a replica signal from a replica generator 2_1. Addition of k products ((Σ 1) through (Σ 4)) is conducted for each sample.

The results of addition are all added by an adder 5_1 to provide an output of the correlator.

The shift registers (1) 1_1-1 to (4) 1_1-4, adders 3_1-1a to 1k, 3_1-2a to 2k, 3_1-3a to 3k, 3_1-4a to 4k, and the replica generator 2_1, can be controlled by control signal.

Operation of each unit when the number of samples is 2, 3, 4 will be described in detail.

When two samples are sampled to one chip, the shift registers (3) 1_1-3, and (4) 1_1-4 are disabled by the control signal. Each of the shift registers (1), (2), (3) and (4) comprises unit block with k elements.

(1, 1, -1, -1, 1, 1, 1, 1, -1, -1, NA, NA, NA, NA, NA, NA, NA, NA, NA, NA) is provided as the replica generator 2_1 wherein NA represent that the state may be any of (1, 0, -1).

The adders (Σ 1) 4-1 and (Σ 2) 4_1-2 are enabled while the adders (Σ 3) 4_1-3 and (Σ 4) 4_1-4 are disabled.

As a result, only signals which are stored in the shift registers (1) 1_1-1 and (2) 1_1-2 are multiplied by replicas (for two samples to one chip) in multipliers 3_1-1a to k

and 3_1-2a to k, respectively and added and output so that an output of the correlator which is equivalent to that of the prior art can be obtained.

When three samples are sampled to one chip, only the shift register (4) 1_1-4 is disabled by the control signal.

(1, 1, 1, -1, -1, -1, 1, 1, 1, 1, 1, 1, -1, -1, -1, NA, NA, NA, NA, NA) is provided as the replica 2_1.

Only the adder (Σ 4) 4_1-1 is enabled.

As a result, only signals stored in the shift registers (1), (2) and (3) are multiplied by a replica 2_1 (three samples to one chip) and the products are added to provide a correlator output.

When four samples are sampled to one chip, all the shift registers (1) to (4) are enabled. (1, 1, 1, 1, -1, - 1, - 1, -1, 1, 1, 1, 1, 1, 1, 1, 1) is provided as the replica 2_1.

The adders (Σ 1) to (Σ 4) are all enabled.

As a result, signals which are stored in the shift registers (1), (2), (3) and (4) are multiplied by replica 2_1 (for four samples to one chip) added to provide an output of the correlator.

In such a manner, the present invention enables the number of samples to be changed to one chip. Accordingly, the shift registers and adders can be selectively used depending upon the number of samples, for example, 1 to 4. Four sample system can be used when better characteristics are required. Four sample system can be converted into two sample system when low power consumption is preferable even if the characteristics are slightly deteriorated. The circuits which are disabled are not supplied with clock signal. This can make the power consumption to a half.

The configuration of an embodied circuit of another correlator of the present invention is shown in Fig. 8.

The sampled input signals are input to the shift registers (1) 1_2-1 to (4) 1_2-4 via a switch 6_2. The length of each of the shift registers is the same as that of spread-code.

In Fig. 8, 4k shift registers are provided so that at most four samples will be sampled.

The switch 6_2 switches the sampled signals every sampling so that the signals are successively input to the shift registers (1) 1_2-1 to (4) 1_2-4.

The signal which is stored in each of shift registers (1) to (4) is multiplied by a replica signal from a replica generator 2_2 and addition (Σ 1) to (Σ 4) of k products (k denotes the spreading factor) is conducted.

The results of addition are all added by an adder 5_2 to provide an output of the correlator.

The shift registers (1) to (4), adders 3_2-1a to 1k, 3_2-2a to 2k, 3_2-3a to 3k, 3_2-4a to 4k, and the replica generator 2_2, can be controlled by control signal.

Operation of each unit when the number of samples is 2, 3, 4 will be described in detail.

When two samples are sampled to one chip, the switch 6_2 alternatively switches the shift registers in response to a control signal so that signals are input to only the shift registers (1) 1_2-1 and (2) 1_2-2. Thus, odd and even number samples are input to the shift registers (1) and (2), respectively.

If it is assumed that the replica signal from the replica generating unit 2_2 is the same as spread-code in the foregoing case, (1, -1, 1, 1, -1) is provided.

The adders (Σ 1) 4_2-1 and (Σ 2) 4_2-2 are enabled while the adders (Σ 3) 4_2-3 and (Σ 4) 4_2-4 are disabled.

As a result, only signals which are stored in the shift registers (1) and (2) are multiplied by replicas in multipliers 3_2-1a to k and 3_2-2a to k, and added by adder 5_2 and output so that an output of the correlator can be obtained.

When three samples are sampled to one chip, the switch 6_2 successively switches the shift registers (1), (2) and (3) so that spread signals are input thereto. On the other hand, the shift register (4) is disabled by its control signal.

Similarly, (1, -1, 1, 1, -1) is provided in the replica generator 2_2.

The adder (Σ 4) 4_2 -4 is disabled.

As a result, only the signals stored in the shift registers (1), (2) and (3) are multiplied by replica signals and the products are added by adder 5_2 and output.

When four samples are sampled for one chip, the switch successively switches the shift registers (1), (2), (3) and (4) in response to a control signal so that spread signals are input thereto.

Similarly, a replica signal (1, -1, 1, 1, -1) is provided in the replica generator 2_2.

As a result, the signals stored in the shift registers (1), (2), (3) and (4) are multiplied by a replica and the products are added by adder 5_2 and output.

In such a manner, the present invention enable the number of samples to be changed to one chip. Accordingly, the shift registers and adders can be selectively used depending upon the number of samples, for example, 1 to 4. Four sample system can be used when better characteristics are required. Four sample system can be converted into two sample system when low power consumption is preferable even if the characteristics are slightly deteriorated. The circuits are not supplied with clock signal when they are to be disabled. This can make the power consumption to a half.

An embodiment of a sample number variable correlator in the direct spread spectrum system using multiplexing will be described with reference to Fig. 9.

In this embodiment, the above-mentioned sampling-number-variable correlator 7 is provided with a control signal generator 8 for determining the number of samples used for demodulation depending upon the number of signals to be multiplexed.

As mentioned above as problems in the prior art, there exists given number of samples, at which a trade off between the characteristics and power consumption is determined by the number of signals to be multiplexed in the multiplexed communication system.

Increasing the number of samples enhances the error rate characteristics while it will aught to an

increase in power consumption. If the present system is used as a portable terminal, etc., the power consumption is a critical factor since it determines the battery drive period of time.

Since the error rate which is generally necessary has been determined, both requirements for decreased power consumption and reduction in error rate can be satisfied by decreasing the number of samples so far as the error rate will not exceed the necessary value.

For example, two, three and four samples are sampled when the number of the signals to be multiplexed is one; two or three; and four or five, respectively.

Combinations of the number of the signals to be multiplexed with the number of samples corresponding to necessary error rates are preliminarily determined. The sampling-number-variable correlator 7 is supplied with a control signal from a control signal generator 8 by providing the number of signals to be multiplexed.

As a result of this, the number of samples can be chosen for each number of signals to be multiplexed so that optimum demodulation can be achieved without wasting power.

Another embodiment of the demodulating device according to the present invention will be described.

The inventors of the present application have proposed a delayed multiplexing method for spreading signals using the same spread-code and a communication system having a non-multiplexed portion (simplex) and a multiplexed portion by using the same method.

In this embodiment, the present invention is applied to a demodulating unit of the system which has been proposed and is characterized in that the number of samples is changed between non-multiplexed and multiplexed portions.

A data format which is used in this embodiment is shown in Fig. 10.

In this case, the number of samples is switched when the non-multiplexed portion is changed to a multiplexed portion.

A case will be described. If information for starting wireless line connection (synchronization signal, packet length, etc.) is inserted in a non-multiplexed portion, it may be desired to reduce error to a low value as less as possible since the information is important.

Accordingly, demodulation is conducted without causing any error by maximizing the number of samples and the characteristics.

Alternatively, the number of samples corresponding to the number of the signals to be multiplexed is selected on the multiplexed portion.

As a result, optimized demodulation can be conducted.

Alternatively, another method using two samples on the non-multiplexed portion can be envisaged.

If the approximately same error rate is required on the non-multiplexed as multiplexed portions, power consumption in the non-multiplexed portion can be reduced by decreasing the number of samples to 2 on the non-multiplexed portion.

The above-mentioned proposal has proposed that data on the number of signals to be multiplexed is embedded in a non-multiplexed portion, so that the number of signals to be multiplexed on the multiplexed portion is demodulated based upon the embedded data. This aims at assuring a transmission rate by flexibly changing the number of signals to be multiplexed depending upon the electromagnetic environment.

Therefore, in accordance with a fixed number of samples are used on non-multiplexed portion and the number of samples is determined on the multiplexed portion, based upon the data embedded in the non-multiplexed portion. The present embodiment is only different from the former embodiment in that the number of signals to be multiplexed has been predetermined while it is embedded in the non-multiplexed portion.

Now, another embodiment of the correlator of the present invention will be described.

Fig. 11 shows the configuration of the circuit of the correlator in the present embodiment in which three samples are sampled to one chip.

In Fig. 11, the three samples 3n+1, 3n+2, 3n+3 (n:0, 1, ..., k) in each of the total k chips, including in a shift register 1_3 is sequentially multiplied by replica signals from a replica generator 2_3 and then the products are added in adders 4_3-1 to 3. One of the results of sums is selected without conducting further adding and is used for demodulation. Since the data is uncertain at its transition position as mentioned above with reference to Fig. 3, an improvement in characteristics can be achieved by using only the result of addition in the correlator, which is obtained by using a sample of three samples in most wide area of the eye pattern.

Sampling at the midpoint of the eye pattern is optimal. However, the timing relationship of sampling is indefinite since sampling is conducted independently of clocking on the transmission side. The timing relationship changes with time due to the difference between clock frequencies on the receiving and transmission sides. Therefore, it is hard to conduct sampling at the midpoint of the eye pattern.

Accordingly, it may be envisaged that better characteristics are obtained by selecting a sample at a wider eye pattern area among samples.

In the present embodiment, only one sample at the most wide area of the eye pattern to one chip is selected out from several samples to one chip.

The selecting method will now be described with reference to Japanese Laid-open Patent Publication (TOKKAI HEI) No. 8-316875 entitled "Clock regenerating circuit" by the inventors of the present application.

Fig. 12 is a block diagram showing a clock regenerating circuit used in the present embodiment.

This circuit will be described below with reference to Fig. 12. Correlation signals from a correlator (not shown in Fig. 12) are spread over a time axis by means of delays 10-1 to 5 (for example, shift registers). It is

assumed that sampling is conducted to sampled two samples to one chip.

The input correlation signal herein may be correlation signal which is determined from all samples in the prior art.

Clock regeneration is conducted by means of synchronization pulses, a window control unit 11 which is controlled by the synchronization pulses and correlation signals of several samples in front of and in rear of the window which is gated by the control unit 11.

The clock is regenerated based upon the synchronization pulses of a synchronization circuit with correlation signals (not shown in Fig. 12). Shift of clocks between transmitting and receiving sides is compensated for by a racking circuit using a window.

The correlation signals in the window (time window) are compared with thresholds which are preset for respective samples by comparators 12-1 to 5, which outputs signals 1 or 0 as the result of the comparison. Thereafter, the output signals are added by means of adders 13-1 to 5. Regenerated clock is controlled by clock regenerator 15 in response to overflow signals from the adders 13-1 to 5.

Fig. 13 shows the clock regenerator 15 shown in Fig. 12.

The clock regenerator 15 generates data clock by dividing the frequency of the sampling clock which has been generated from the synchronization pulse generating circuit 15g and used for despreading by $2 \times k$ frequency divider 15d-2 (k denotes the spread-code length). It is necessary to control the data clock since there is an incorrect timing relationships between clock signals on the transmitting and receiving sides.

Control is carried out in this example as follows: When the adder 13-3 of the midpoint timing of the window is previously overflown, the current timing relationship of the clock regenerator 15 (clock which is generated by $2 \times k$ frequency divider 15d-2) is maintained while the timing relationship of the clock regenerator 15 is delayed by one step (clock which is generated by $2 \times k$-1 frequency divider 15d-1) when the adder of the earlier timing relationship is overflown.

On the other hand, the timing relationship of the clock regenerator 15 is advanced by one step (clock generated by $2 \times k+1$ frequency divider 15d-3) when the adder of the late timing relationship is previously overflown. Tracking of regenerated clock is conducted in such a manner.

Alternative methods of shifting the timing relationship by two samples, weighing method, adding by every sample, etc. are proposed.

The circuit configuration for carrying out the selecting method using this clock regenerating circuit is shown in Fig. 14.

In the receiver, I and Q signals are separately sampled by sampling means (not shown) and are input to the correlator in the embodiment of the present invention shown in Fig. 11.

Although three outputs are output from the correlator as output addition signal for three samples, two outputs are output in the case of two samples.

The addition signal on three channels which is output from the correlator in such a manner is divided into two signals so that one is input to switching circuits 20i, 20q and the other is input to adders 21i, 21q for adding signals on three channels.

A signal representing an absolute value of the amplitude (referred to as MAG signal) is generated by calculating the root of the sum of the squares of I and Q addition signals by a root-of-sum-of-squares circuit 22 and is input to the above-mentioned clock regenerating circuit 23.

The clock regenerating circuit 23 conducts comparison between previous and subsequent correlation outputs for holding clock signals as mentioned above.

Now, the selecting method will be described in case of two and three samples.

The method in case of two samples is shown in Fig. 15.

In this case, two samples are sampled to one chip. The sampling timing relationships I and II, different each other, are illustrated.

In the timing relationship I, sampling is conducted at [1], [2], [3], [4].

On the other hand, an addition result, that is sum of correlation outputs at [1] and [2] is obtained at A in the clock regenerating circuit 23. An addition result of correlation outputs at [2] and [3] is obtained at B. An addition result of correlation output [3] and [4] is obtained at C. Accordingly, the MAG outputs which are addition outputs are obtained with its amplitude as shown at (a), (b) and (c). A clock signal at B is held.

In this case, a sample corresponding to a larger area of the eye pattern is selected among samples [2] and [3].

Since the MAG output (a) is a sum of the correlation outputs at sampling times [1] and [2] and no timing relationship is established at [1], its amplitude is substantially zero. Correlation is established at [2], but the sample is in the narrow area of the eye pattern and its amplitude is so low that its correlation output is low in proportion with the amplitude of the sample.

On the other hand, the MAG output (c) is a sum of the correlation outputs at [3] and [4] and no correlation is established at [4] and the amplitude of the output at C is substantially zero. A correlation is established at [3] and the eye of the eye pattern is largely opened and its correlation output is larger in proportional to the amplitude of the sample [3].

As a result, comparison between the MAG outputs (a) and (c) shows that the output (c) is larger.

Although the sample (a) may sometimes become larger than the sample (c) and vice versa due to occasional data and/or noise, the sample (c) can be made always larger by subjecting the samples to an integration for a given period of time.

In the timing relationship II, sampling is conducted at [5], [6], [7], [8].

On the other hand, an addition result of correlation outputs at [5] and [6] is obtained at D in the clock regenerating circuit 23. An addition result of correlation outputs at [6] and [7] is obtained at E. An addition result of correlation output [7] and [8] is obtained at F. Accordingly, the MAG outputs which are addition outputs are obtained with its amplitude as shown at (d), (e) and (f). A clock signal at E is held.

In this case, a sample corresponding to a larger area of the eye pattern is selected among samples [6] and [7].

Since the MAG output (d) is a sum of the correlation outputs at sampling times [5] and [6] and no timing relationship is established at [5], its amplitude is substantially zero. Correlation is established at [6], but the sample is in the larger area of the eye pattern.

On the other hand, the MAG output (f) is a sum of the correlation outputs at [7] and [8] and no correlation is established at [8] and the amplitude of the output is substantially zero. A correlation is established at [7] and the eye of the eye pattern is smaller and its correlation output is smaller in proportional with the low amplitude of the sample.

As a result, comparison between the MAG outputs (d) and (f) shows that the output (d) is larger.

In such manner, the selecting circuit of the present invention compares the MAG outputs which are previous and subsequent of the sampling time to which the clock regeneration is referenced and selects a larger MAG output. If the previous output is larger, the previous sample of two samples would be closer to the center area of the eye pattern. If the subsequent output is larger, the subsequent sample of two samples is closer to the center area of the eye pattern.

The selecting circuit 24 switches switching circuits 20i, 20q to select samples used for demodulation in such a manner.

The method in case of three samples is shown in Fig. 16.

The sampling timing relationships I and II, different each other, are also illustrated.

In the timing relationship I, sampling is conducted at [1], [2], [3], [4] and [5].

On the other hand, an addition result of correlation outputs at [1], [2] and [3] is obtained at A in the clock regenerating circuit. An addition result of correlation outputs at [2], [3] and [4] is obtained at B. An addition result of correlation output [3], [4] and [5] is obtained at C. Accordingly, the MAG outputs which are addition outputs are obtained with its amplitude as shown at (a), (b) and (c). A clock signal at B is held.

In this case, a sample corresponding to a larger area of the eye pattern is selected among samples [2], [3] and [4].

Since the MAG output (a) is a sum of the correlation outputs at sampling times [1], [2] and [3] and no timing relationship is established at [1], its amplitude is substantially zero. Correlation is established at [2] and [3].

On the other hand, the MAG output (c) is a sum of the correlation outputs at [3], [4] and [5] and no correlation is established at [5] and the amplitude of the output is substantially zero. A correlation is established at [3] and [4].

The MAG output (b) is a sum of the correlation outputs at [2], [3] and [4] and a correlation is established.

When an odd number of samples are sampled, the time at which the amplitude of the eye pattern is largest is coincident with the time of clock regeneration.

As a result, sampling in the timing relationship of clock regeneration is selected by the selecting circuit 24.

In the timing relationship II, sampling is conducted at [6], [7], [8], [9] and [10].

An addition result of correlation outputs at [6], [7] and [8] is obtained at D. An addition result of correlation outputs at [7], [8] and [9] is obtained at E. An addition result of correlation output [8], [9] and [10] is obtained at F. Accordingly, the MAG outputs which are addition outputs are obtained with its amplitude as shown at (d), (e) and (f). A clock signal at E is held.

When an odd number of samples are sampled, the time at which the amplitude of the eye pattern is largest is coincident with the time of clock regeneration.

As a result, sampling in the timing relationship of clock regeneration is selected by the selecting circuit 24.

Also in this case, the time when the amplitude of the eye pattern is highest is coincident with the time of clock regeneration.

As a result, the selecting circuit 24 selects sampling at time of clock regeneration.

Only a sampled signal which corresponds the highest amplitude of the eye pattern can be selected among independently sampled signals in accordance with the present invention.

As a result, an improvement in error rate characteristics can be achieved in comparison with the case in which all samples are added.

Although the invention has been described with reference to only embodiments using two and three samples, the present invention can be equally embodied by using four, five samples, etc.

If an even number of samples are sampled, a larger sample is selected by comparing the MAG outputs at times before and after the center of the clock regeneration, similarly to the case of two samples. If the previous sample is larger than the subsequent sample, the previous sample is selected. If subsequent sample is larger, this sample is selected.

In case of four samples, the two samples which are previous and subsequent to consecutive two samples may be compared to each other since two consecutive samples give an influence to the previous and subsequent samples. This case is illustrated in Fig. 17.

This case is a case of sampling of an even number of samples in which four samples are sampled to one chip.

Sampling is conducted at [1], [2], [3], [4], [5], [6], [7] and [8].

On the other hand, in the clock regenerating circuit 23, the addition result of the correlation outputs at [1], [2], [3] and [4] is output at A, the addition result of the correlation outputs at [2], [3], [4] and [5] is output at B, the addition result of the correlation outputs at [3], [4], [5] and [6] is output at C, the addition result of the correlation outputs at [4], [5], [6] and [7] is output at D, and the addition result of the correlation outputs at [5], [6], [7] and [8] is output at E. The MAG outputs which are addition outputs with its amplitude as shown at (a), (b), (c), (d) and (e). A clock signal is held at C.

A sample which corresponding to the highest amplitude of the eye pattern is also selected from the samples at [3], [4], [5], [6] in this case. The samples [4] and [5] are in the vicinity of the midpoint of the eye pattern.

Since the subsequent MAG output is larger, subsequent sample, that is sample at [5] will be selected.

Alternatively, two samples may be selected from four samples. In this case, samples at [4] and [5] may be selected.

Only two samples at [4] and [5] of the selected results are added and used for demodulation.

It is understood that this method can be equally used in case of an even number of samples.

On the other hand, when an odd number of samples are sampled, a sample corresponding to the midpoint of the eye pattern can be selected by using the timing relationship of the clock regeneration.

An example of sampling of 5 samples is illustrated in Fig. 17.

Sampling is conducted at [9], [10], [11], [12], [13], [14], [15] [16], [17] and [18].

On the other hand, in the clock regenerating circuit 23, the addition result of the correlation outputs at [10], [11], [12], [13] and [14] is output at F, the addition result of the correlation outputs at [11], [12], [13], [14] and [15] is output at G, the addition result of the correlation outputs at [12], [13], [14], [15] and [16] is output at H, the addition result of the correlation outputs at [13], [14], [15], [16] and [17] is output at I, and the addition result of the correlation outputs at [14], [15], [16], [17] and [18] is output at J. The MAG outputs which are addition outputs with its amplitude as shown at (f) to (l). A clock signal is held at H.

A sample corresponding to the highest amplitude of the eye pattern is also selected from the samples at [12], [13], [14], [15] and [16] in this case.

Also in this case, the time when the amplitude of the eye pattern is highest is coincident with the time of clock regeneration.

As a result, sampling in the timing relationship if clock regeneration is selected by the selecting circuit 24.

In such a manner, the clock regeneration timing relationship may be used for three (odd number) samples sampling to one chip.

If three samples, etc. are used of five samples, the results of selection at [13], [14] and [15] are added and used for demodulation.

The correlator for extracting data from the serial type shift registers shown in Fig. 11 each time of sampling in the foregoing description, further embodiments are illustrated in Figs. 18 and 19.

An correlator which carries out addition each time of sampling is shown in Fig. 18.

Although addition is conducted in the exemplified embodiment of Fig. 11 at each sample to one chip and addition operations (3m+1), (3m+2), (3m+3) are separately performed, an equal operation result can be obtained by performing addition every other sample or samples.

The value which is stored in the shift register 13_4 at t is shifted by one sample at t+1.

For example, if an addition of (3m+1) is performed at t by performing every three samples, an output of (3m+2) can be obtained from an adder 4_4. As result which is equal to that of Fig. 11 is obtained.

A method of using a parallel type of correlator as shown in Fig. 8 is used is shown in Fig. 19.

Since results of addition of each block of samples are output in a parallel manner in this case, they can be directly used.

The addition results Σ1, Σ2, Σ3, Σ4 of respective adders 4_5-1 to 4 are sums of every samples. Thus, an equal result can be obtained by using this.

Since a total sum of Σ1, Σ2, Σ3, Σ4 is required for clock regeneration per se, the total sum can be obtained as an correlation output by adding these four sums.

Now, another embodiment of the clock regenerating circuit of the present invention will be described.

The clock regenerating signal is used without processing it in the foregoing embodiment.

For example, when an odd number of samples are sampled, selection is performed with reference to the timing relationship which is identical to the clock regeneration timing relationship.

However, the value at which overflow of the adder in Fig. 12 occurs is often preset considerably larger for eliminating variations due to noise and/or phasing since the clock error between the transmitter and receiver is adjusted by the clock regenerating circuit and the clock signal on only either one of the transmitter and receiver is certainly advanced and the same shift of clock frequency occurs.

It is an object of the clock regeneration per se to regenerate correct clock signals rather than to capture the center of the eye pattern.

The present embodiment has a feature, as shown in Fig. 20, that the adders 13-1 to 5 of the clock signals are separate from the selecting adders 16-1 to 3 so that their overflow can be changed.

Changes in amplitude of the eye pattern and the manner of switching is shown in Fig. 21.

① and ② denote changes in amplitude of the eye pattern in adjacent timing relationships.

As shown in a part (a) of Fig. 21, the eye pattern in the timing relationship ② becomes larger in amplitude with lapse of time and exceeds it at time [A] due to shift of clock signals.

It is ideal that switching occur at [A]. Since an integration operations are performed in adders for eliminating clock changes due to noise and/or phasing, the eye patterns can not be quickly switched.

A case in which the integration period of time is longer is shown in a part (b) of Fig. 21.

The integrated value of ① (right hand hatched area) is larger than that of ② (left hand hatched area) even at time [D]. The integrated value ② becomes larger than that of ① at time [B] at last.

On the other hand, a case in which the integration period of time is made shorter is shown in a part (c) of Fig. 21. In this case, since the integration period of time is shorter, the addition result of ② becomes larger at [C]. It is possible to switch earlier.

Since the integration period of time is larger to keep stability in the clock regenerating circuit, the time of switching is inevitably late, resulting in a switching timing relationship as shown in a part (b) of Fig. 21.

Therefore, the present invention decreases the number of integration operations by providing adders which are devotedly used for selecting to provide the characteristics to enable rapid switching.

Although the present embodiment has been described with reference to the clock regenerating circuit comprising adders using comparators, the present embodiment can be modified to change the integration load in all integration methods used in the clock regenerating circuit which was invented by the present inventors.

A further embodiment will be described.

Although the above embodiment has a feature that the number of integration operations performed in adders is changed in the clock regenerating circuit, the number of integration operation may be externally controlled depending upon transmission rate.

As is generally known, the quartz crystal oscillators having a stability of several ppm to about 100 ppm used for generating clock are commercially available. Their stability is selected depending upon application.

If 10 MHz is obtained by a quartz crystal oscillator having a frequency stability of 10 ppm, the frequency offset would be 100 Hz.

If sampling is conducted at 10 MHz, the sample may be shifted to adjacent sample after sampling of 100,000 samples.

Accordingly, the number of integration operations is changed in view of it.

A frequency of 1 MHz which is obtained by dividing the frequency from a 10 MHz oscillator is used for sampling some systems. In this case, a sample may be shifted to adjacent sample after sampling of 10,000 samples.

In such a manner, an optimal integration load differs depending upon the stability of used oscillator, frequency, sampling frequency, data rate, spreading rate, etc.

Hence, the present embodiment has a feature that the integration load is preliminarily preset based upon these parameters and the integration load is changed depending upon the use conditions.

In the communication system, data rate, spreading rate, etc. are changed. Optimal switching can be performed by changing the number of integration times depending upon these parameters.

A further embodiment of the clock regenerating circuit of the present invention will be described. The present inventors of the present application have proposed an invention for eliminating cross interference on duplexing in a delayed multiplexing system (Japanese Patent Application No. 8-47118).

The proposed invention aims at eliminating interference by blocking the multiplexed signals, using the correlation values therebetween and performing operation on the values.

Accordingly, in order to improve the characteristics, it is required that there is not rapid changes between blocked signals.

On the other hand, the sampling timing relationship which is selected when the integrated value becomes a constant if the clock regeneration is used or said adders are used.

Accordingly, the sampling timing relationship is changed for a period of blocked signals, resulting in a deterioration on demodulation.

Therefore, the present invention has a feature that the time of switching of the selected sampling is changed at a transition of each block of signals.

This configuration is illustrated in Fig. 22.

In a demodulating system for spread spectrum communication, a correlation synchronizing circuit is always necessary in addition to the clock regenerating circuit so that synchronization of correlation is established.

The correlation synchronizing circuit has a correlation symbol counter, the leading edges of blocked signals can be detected.

Switching of selecting circuits can be conducted each block of signals by controlling the timing relationship in response to a signal from the symbol counter.

As a result, switching of selecting circuits is conducted each in unit of block so that reduction in cross interference on multiplexing in the multiplexing system which is proposed by the present inventors, is effectively achieved.

A further embodiment will be described.

In the above-mentioned embodiment, a method of selecting the number of samples has been described

and a method of selecting one or in samples from several samples to one chip has been described.

Optimal characteristics can be obtained at an optimum power consumption by determining the number of samples depending upon the number of signals to be sampled and selecting one sample or m samples among the determined number of samples.

Advantageous effects according to the present invention as follows:

(1) The demodulating device of the present invention can be operated by sampling a given number of samples in view of power consumption and characteristics due to the fact that the device has means for changing the number of samples in response to a control signal. A communication system which is optimal for mobile application can be built.

(2) The correlator of the present invention controls each of components depending upon the number of samples when correlation processing is performed by using a method in which the shift registers for distributing received spread signal inputs are in series connected to each other or a method in which the shift registers, each for several samples are in parallel connected to each other. Therefore, a system in which reduction in power consumption can be achieved by changing the number of samples depending upon the characteristics can be built.

(3) In addition to the advantageous effect of (1) mentioned above, optimal characteristics can be obtained by changing the number of samples to be controlled depending upon the multi-valued number if transmitted signal has a multi-valued signal level in which several spread signals are added as is done in code division multiplexing.

(4) In addition to advantageous effect of (1) mentioned above, optimal characteristics can be obtained at both non-multiplexed and multiplexed portions by switching the number of samples between non-multiplexed portion and multiplexed portion in a system for transmitting plural series of signals which are multiplexed by delaying, the desired several chips by desired several chips, signals which are spread with the same spreading code as that of a non-multiplexed portion in a data format. Alternatively, signals carrying the number of signals to be multiplexed may be transmitted and the number of signals to be multiplexed is identified on the receiving side. The number of samples can be switched from the multiplexed portion depending upon the identified number of signals to be multiplexed.

(5) Demodulation can be performed only in an region having a better C/N ratio by using one sample or m samples per chip of signals which are sampled by sampling several samples (k samples) (k>m) per one chip. This results in reduction in error rate on demodulation.

(6) In addition to advantageous effect of (5) mentioned above, using a clock regenerating circuit for regenerating clock as means for selecting sample signals makes it possible to select much better region having a much better C/N ratio.

A circuit can be commonly used by obtaining the despread signals by adding signals which are despread one sample by one sample.

(7) In addition to advantageous effects of (6) mentioned above, if an even number of samples (for example, two samples per one chip) are sampled, a larger MAG output is selected from previous and subsequent samples with respect to the midpoint of an eye pattern. A sample which is in a region having a better C/N ratio of an eye pattern can be positively selected by selecting previous or subsequent sample if the previous sample is larger than the subsequent sample or vice versa.

(8) In addition to advantageous effect of (6) mentioned above, if an odd number of samples (for example, three samples per one chip) are sampled, a region of an eye pattern having a better S/N ratio can be positively selected by performing sampling in the timing relationship of clock regeneration.

(9) In addition to advantageous effects of (6) to (8) mentioned above, the integration for selection can be switched more rapidly by being replaced with the integration for clock regeneration.

The number of integration operations can be switched depending upon the system with reference to the accuracy of the oscillator used for the communication system, data rate and spreading rate.

(10) In addition to advantageous effects of (6) to (9) mentioned above, cancellation of cross interference can be performed in an excellent manner by selecting each unit of multiplexed block in a system in which transmitted and received signals are multiplexed.

(11) A system having a low power consumption and excellent characteristics can be built by combining a method of selecting signals used for demodulation from sampled signals with the method of selecting the number of samples by means of the demodulating device of the present invention.

Claims

1. A demodulating device in the direct spread spectrum communication system having sampling means for sampling a given number of samples to one chip from input spread signals in a base band area, which are directly spread with a spread-code, the demodulating device being adapted to perform despreading based upon discrete sample signals which are obtained by the sampling means for demodulation, characterized in that the sampling

means in which the number of samples can be controlled in response to a control signal is used.

2. A correlator in the direct spread spectrum communication system having sampling means for sampling a given number of samples to one chip from input spread signals in a base band area, which are directly spread with a spread code, the correlator being adapted to determine a correlation between discrete sample signals by multiplying discrete sample signals which are obtained by the sampling means by a reference spread signal prepared relevant to one code-length of the spread-code for said discrete sample signals and by adding the results of multiplication in each chip when demodulation is performed by conducting despreading based upon the discrete sample signals, characterized in that the correlator comprises a number of in-series-connected shift registers (1_1-1 to 4, 1_3, 13_4) being inputted the discrete sample signals, the number of which is equal to the maximum number of samples to one chip and replica signal generating means (2_1, 2_3, 23_4) for generating a number of replica signals, the number of which is equal to the number of samples to the same chip as replica of the reference spread signal.

3. A correlator in the direct spread spectrum communication system having sampling means for sampling a given number of samples to one chip from input spread signals in a base band area, which are directly spread with a spread code, the correlator being adapted to determine a correlation between discrete sample signals by multiplying discrete signals which are obtained by the sampling means by a reference spread signal prepared relevant to one code-length of the spread-code for said discrete sample signals and by adding the results of multiplication in each chip when demodulation is performed by conducting despreading based upon the discrete sample signals, characterized in that the correlator comprises a number of in-parallel-connected shift registers (1_2-1 to 4, 1_5-1 to 4) being inputted the discrete sample signals, the number of which is equal to the maximum number of samples to one chip and replica signal generating means (2_2, 23_5) for generating a number of replica signals, the number of which is equal to the number of samples to the same chip as replica of the reference spread signal.

4. A demodulating device in the direct spread spectrum communication system as defined in Claim 1, characterized in that a control signal is generated (8) for controlling the number of samples depending upon the multi-valued number which the signal level of the input spread signals has.

5. A demodulating device in the direct spread spectrum communication system as defined in Claim 1, characterized in that when a signal in a predetermined data format including a non-multiplexed portion containing data for defining the communication format, which is followed by a multiplexed portion is input as the input spread signals, a control signal for controlling the number of samples, which is preset in the non-multiplexed portion, or a control signal for controlling the number of samples depending upon the multi-valued number which the signal level of multiplexed spread signal has in the multiplexed portion is generated (8) as a control signal for controlling the number of samples.

6. A demodulating device in the direct spread spectrum communication system as defined in Claim 4, characterized in that when a signal in a predetermined data format including a non-multiplexed portion containing data for defining the communication format, which is followed by a multiplexed portion is input as the input spread signals, a control signal for controlling the number of samples is generated (8) by using a multi-valued number which is obtained by identifying the multi-valued number which has been incorporated in the non-multiplexed portion.

7. A demodulating device in the direct spread spectrum communication system having means for sampling a given number of samples to one chip from input spread signals in a base band area, which are directly spread with a spread-code, the demodulating device being adapted to perform despreading based upon discrete sample signals which are obtained by the sampling means for demodulation, characterized in that the demodulating device comprises sample signal selecting means (20_i, 20_q, 24) for selecting a number of samples, the number of which is less than a given number of samples of each chip from the discrete sample signals which are obtained by sampling of the sampling means to despread only sample signals which are selected by said sample signal selecting means for demodulation.

8. A demodulator device in the direct spread spectrum communication system as defined in Claim 7, characterized in that the sample signal selecting means (20_i, 20_q, 24) selects sample signals in such a timing relationship that a correlation signal is generated, which is detected in a clock regenerating circuit (23) for regenerating sampling clock signals based upon despread signals which are obtained by adding correlation signals based on all sample signals which are sampled by the sampling means.

9. A demodulating device in the direct spread spec-

trum communication system as defined in Claim 8, characterized in that the despread signals which are obtained by adding correlation signals based on the all sample signals are obtained by adding signals which are obtained by despreading sample by sample a given number of sample signals of each chip, which are obtained by the sampling means.

10. A demodulator device in the direct spread spectrum communication system as defined in Claim 8 or 9, characterized in that when despreading is performed by sampling an even number of samples to one chip and by using a passive type of correlator, a sample signal is selected which corresponds to larger one of previous and subsequent correlation MAG outputs with respect to the midpoint of a timing interval in which correlation signals which are detected by the clock regenerating circuit (23) are generated.

11. A demodulator device in the direct spread spectrum communication system as defined in Claim 8 or 9, characterized in that when despreading is performed by sampling an odd number of samples to one chip and by using a passive type of correlator, discrete sample signals are selected in a clock timing relationship in which correlation signals which are detected by the clock regenerating circuit (23) are generated.

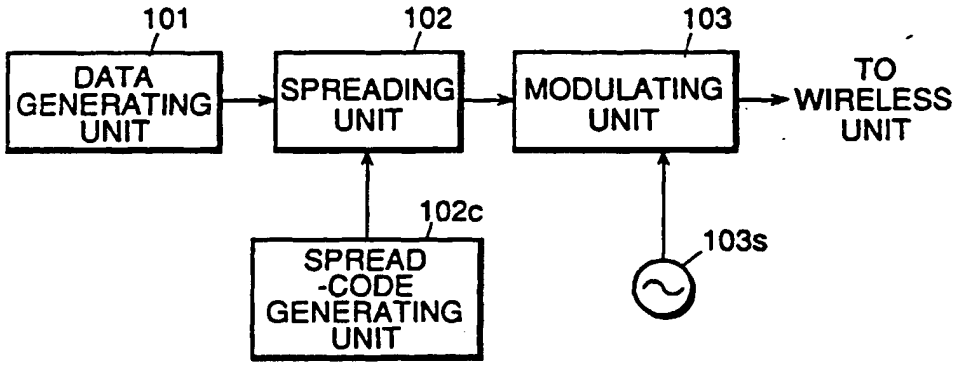
12. A demodulating device in the direct spread spectrum communication as defined in any one of Claims 8 to 11, characterized in that the clock regenerating circuit (23) comprises correlation signal integrating means for detecting the timing relationship in which correlation signal are generated and integrating means for selecting sample signals, which is separate from the integrating means for clock generating.

13. A demodulating device in the direct spread spectrum communication system as defined in Claim 12, characterized in that the number of integration operations depending upon the discrete sample signals which are performed in the integrating means for selecting sample signals is determined and preset as a function of data rate and spreading rate, based upon the accuracy of an oscillator used in the communication system.

14. A demodulating device in the direct spread spectrum communication system as defined in any one of Claim 7 to 13, characterized in that when signals which have been spread by using the same spread-code, delayed and multiplexed are input as the input spread signals, the sample signals which are selected depending upon the operation of the sample signals are changed each block unit of the delayed and multiplexed signals so that the condition of selecting of the sample signals is maintained for a period of the block unit.

15. A demodulating device in the direct spread spectrum communication system characterized in that the sampling means of the demodulator device in the direct spread spectrum communication system as defined in any one of Claims 1, 4, 5 and 6 is used as sampling means of the demodulating device in the direct spread spectrum communication system as defined in any one of Claims 7 to 14.

FIG.1
(PRIOR ART)



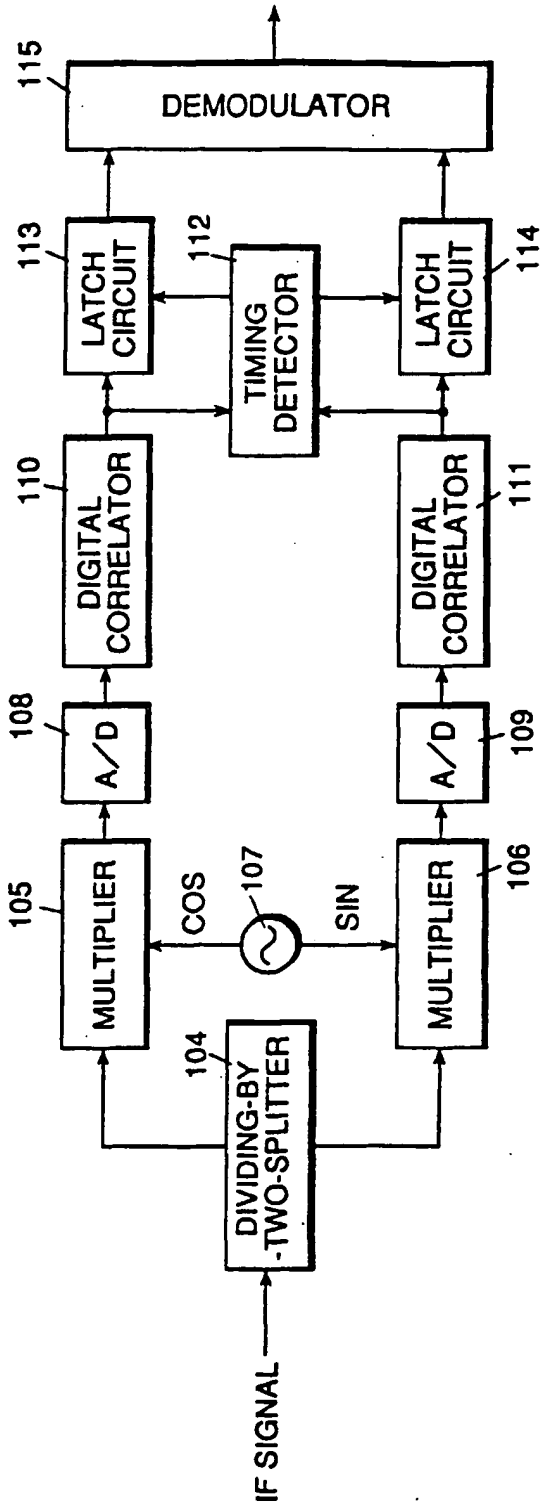


FIG.2
(PRIOR ART)

FIG.3
(PRIOR ART)

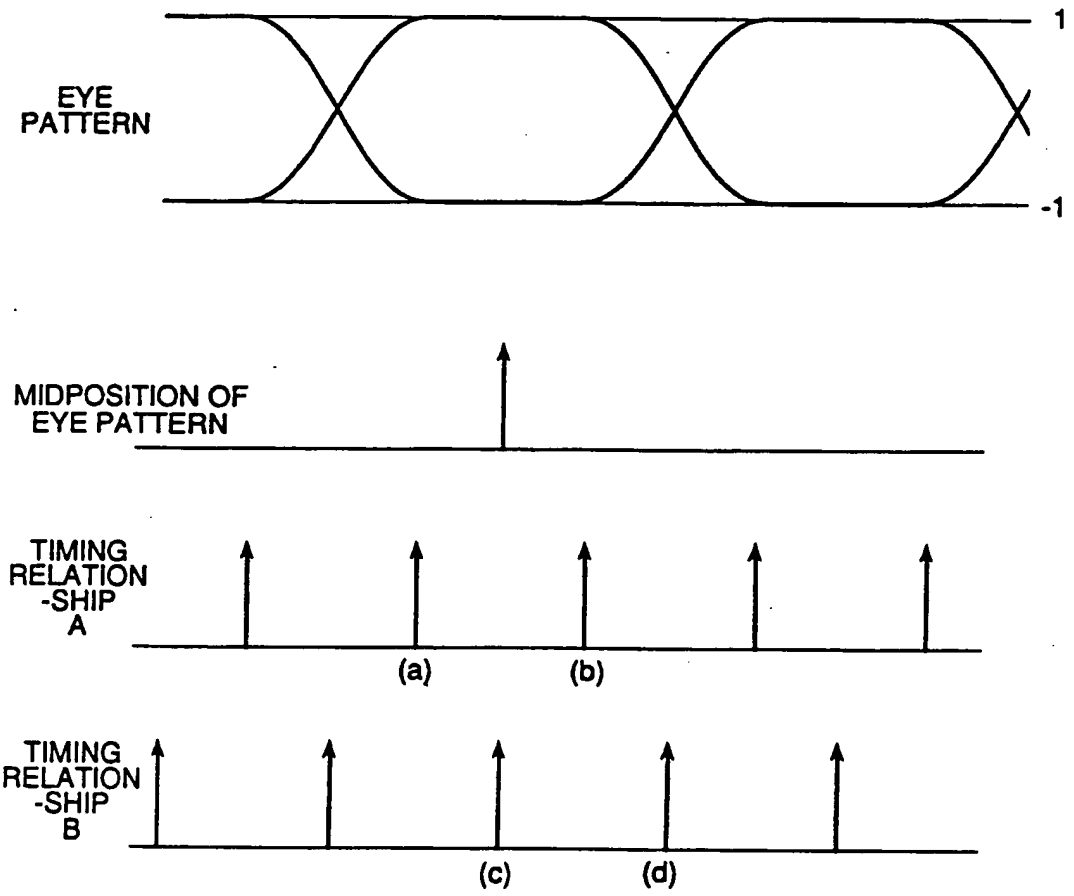


FIG.4
(PRIOR ART)

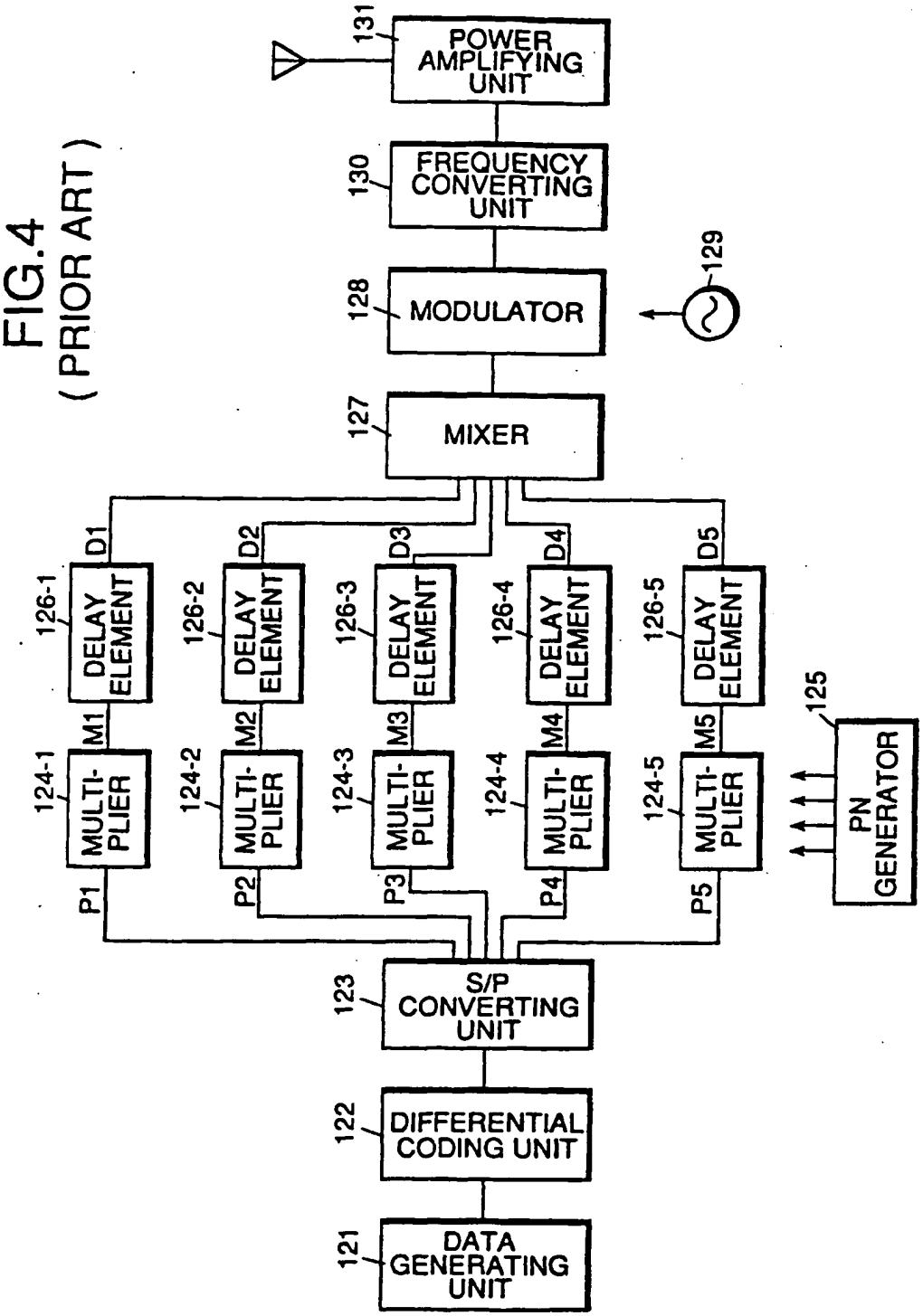


FIG.5
(PRIOR ART)

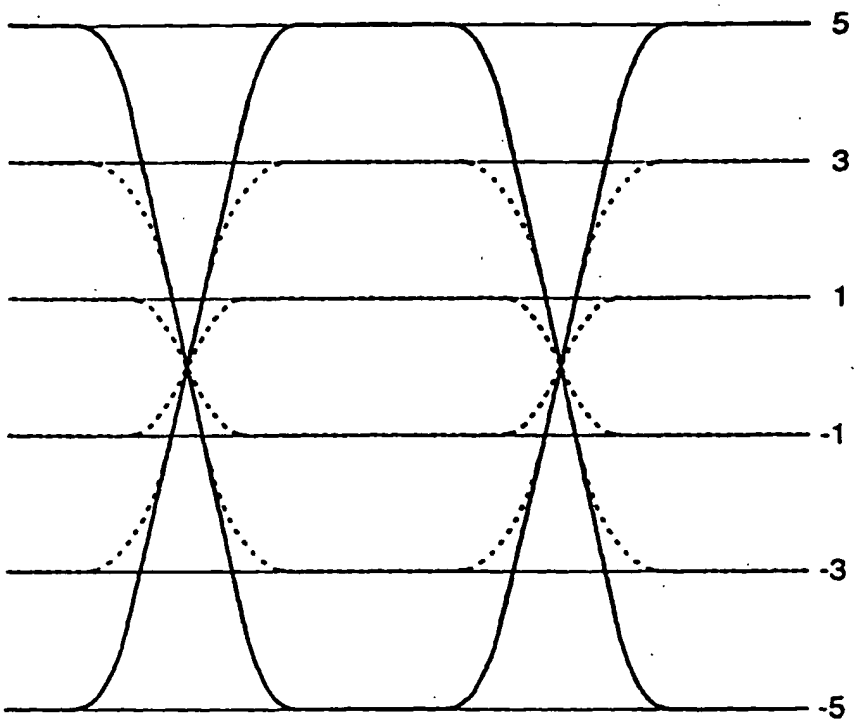


FIG.6
(PRIOR ART)

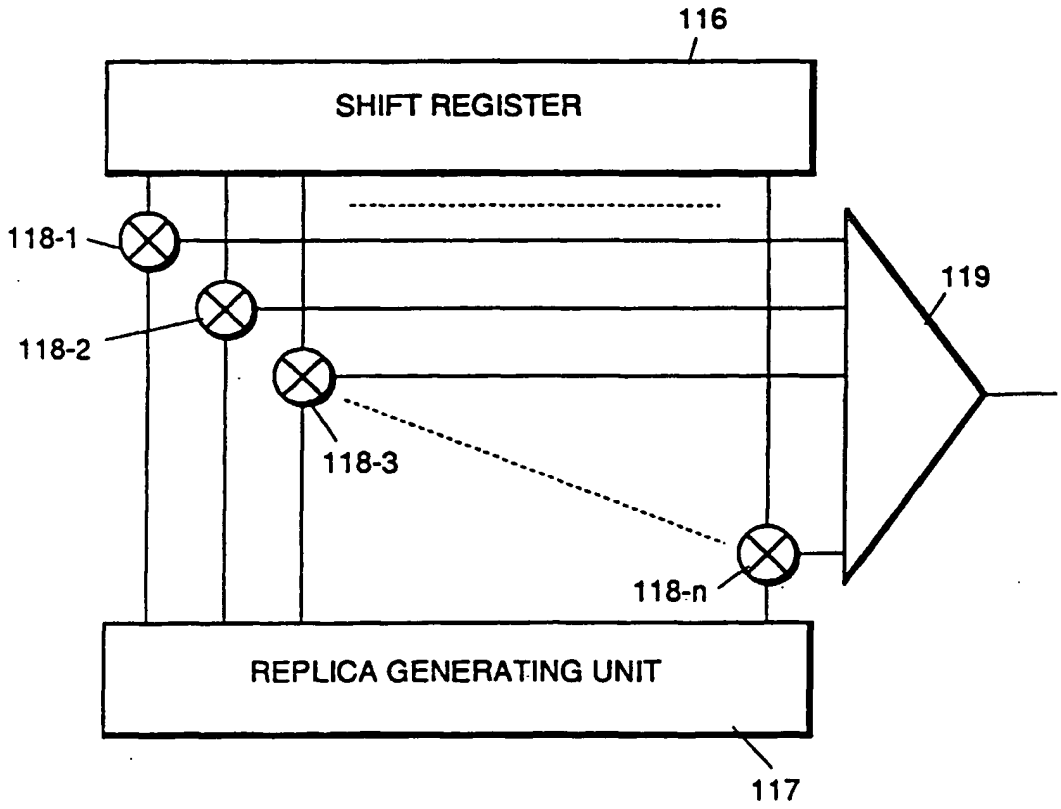


FIG.7

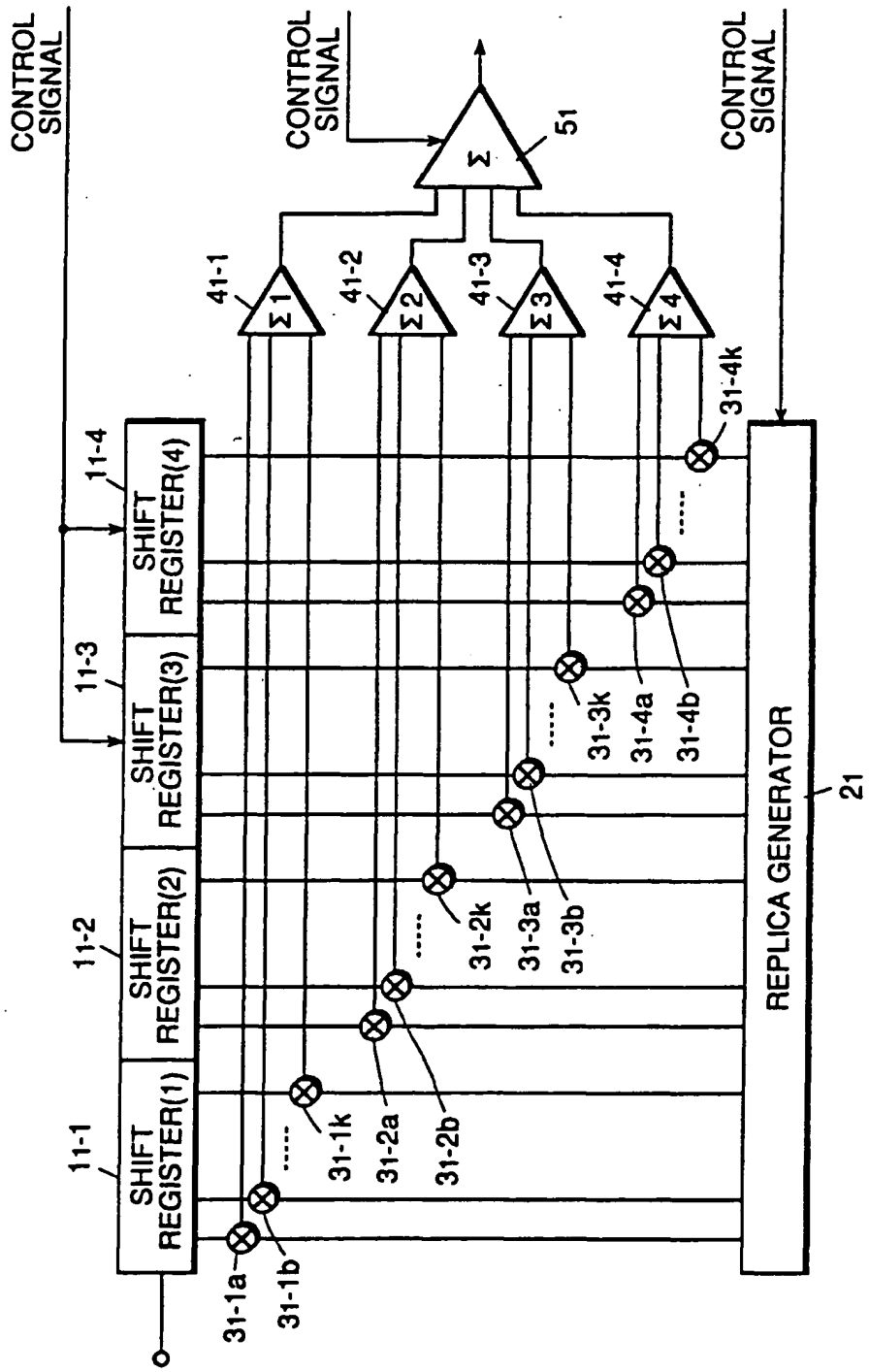

CONTROL SIGNAL
CONTROL SIGNAL
CONTROL SIGNAL
Σ
51
41-1
Σ1
41-2
Σ2
41-3
Σ3
41-4
Σ4
11-1
SHIFT REGISTER(1)
11-2
SHIFT REGISTER(2)
11-3
SHIFT REGISTER(3)
11-4
SHIFT REGISTER(4)
31-1a
31-1b
31-1k
31-2a
31-2b
31-2k
31-3a
31-3b
31-3k
31-4a
31-4b
31-4k
REPLICA GENERATOR
21

FIG.8

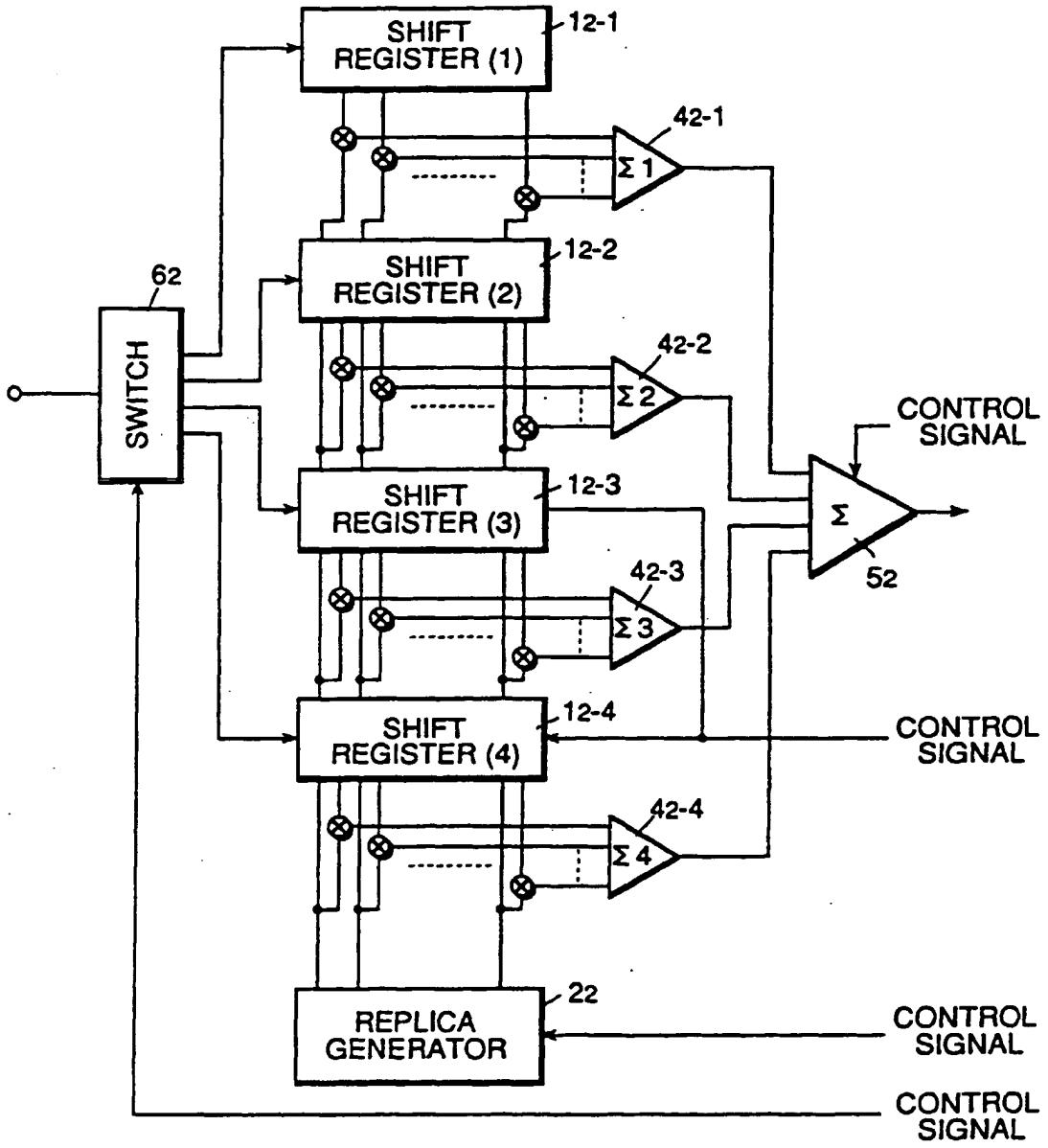

SHIFT REGISTER (1)
12-1
42-1
Σ 1
SHIFT REGISTER (2)
12-2
62
SWITCH
42-2
Σ 2
CONTROL SIGNAL
SHIFT REGISTER (3)
12-3
Σ
52
42-3
Σ 3
SHIFT REGISTER (4)
12-4
CONTROL SIGNAL
42-4
Σ 4
REPLICA GENERATOR
22
CONTROL SIGNAL
CONTROL SIGNAL

FIG.9

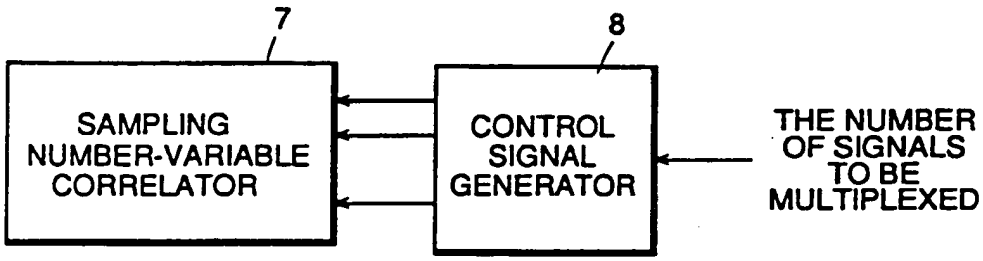

7
8
SAMPLING NUMBER-VARIABLE CORRELATOR
CONTROL SIGNAL GENERATOR
THE NUMBER OF SIGNALS TO BE MULTIPLEXED

FIG.10


NON-MULTIPLEXED PORTION
MULTIPLEXED PORTION

FIG.11

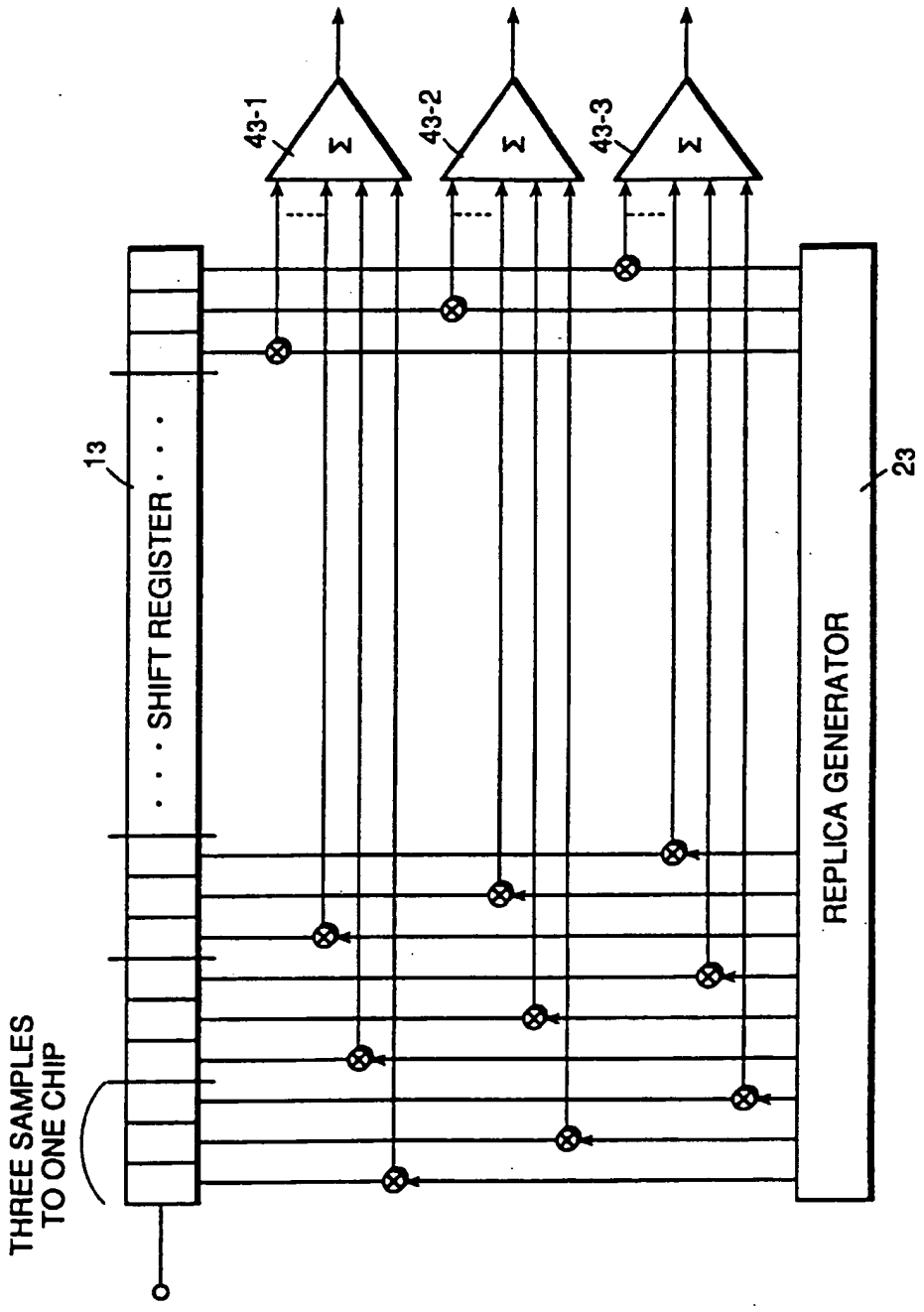

43-1
43-2
43-3
Σ
13
SHIFT REGISTER
23
REPLICA GENERATOR
THREE SAMPLES
TO ONE CHIP

FIG.12

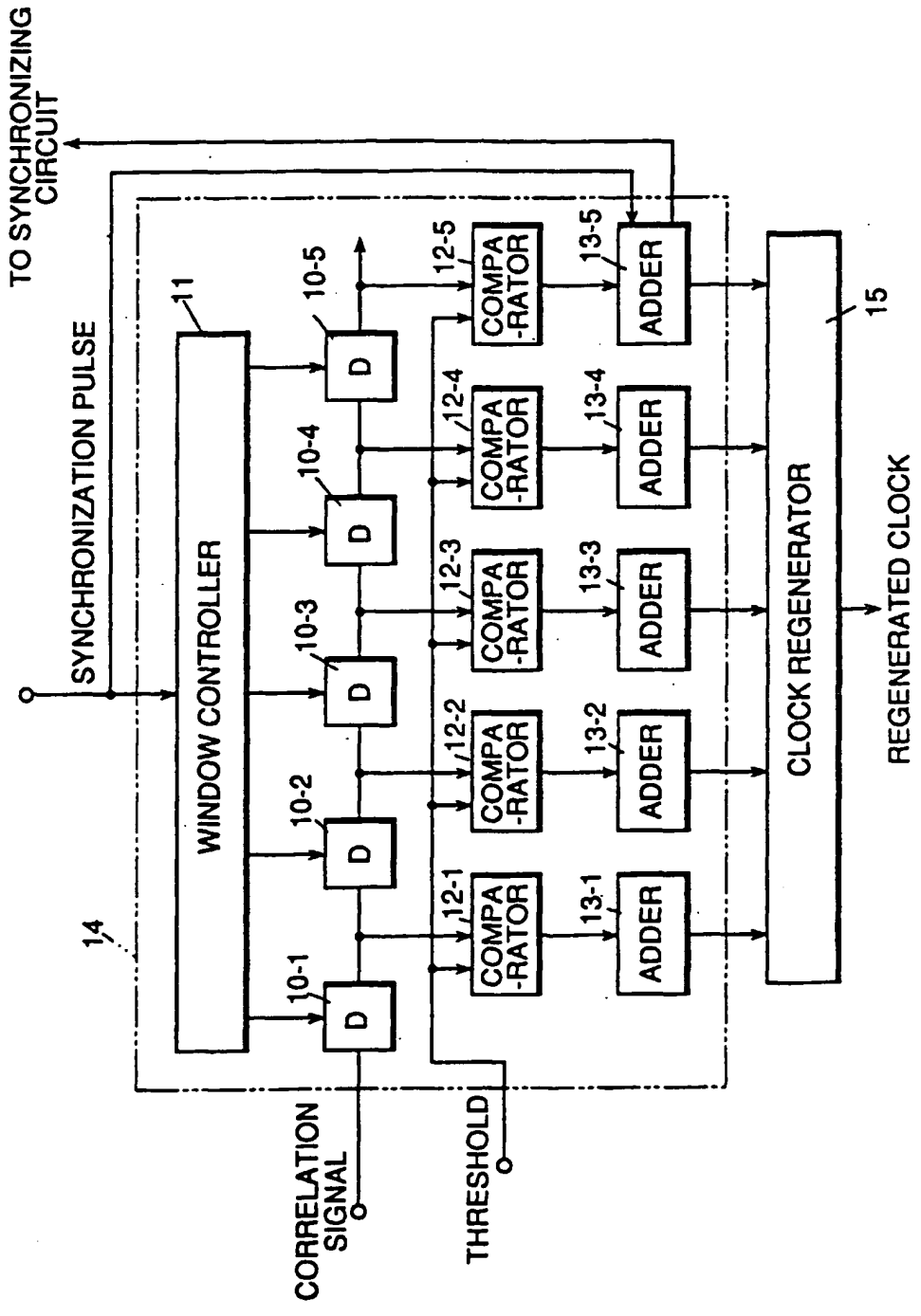

TO SYNCHRONIZING CIRCUIT
SYNCHRONIZATION PULSE
WINDOW CONTROLLER
11
14
10-1
10-2
10-3
10-4
10-5
D
12-1
12-2
12-3
12-4
12-5
COMPA-RATOR
13-1
13-2
13-3
13-4
13-5
ADDER
CLOCK REGENERATOR
15
REGENERATED CLOCK
CORRELATION SIGNAL
THRESHOLD

FIG.13

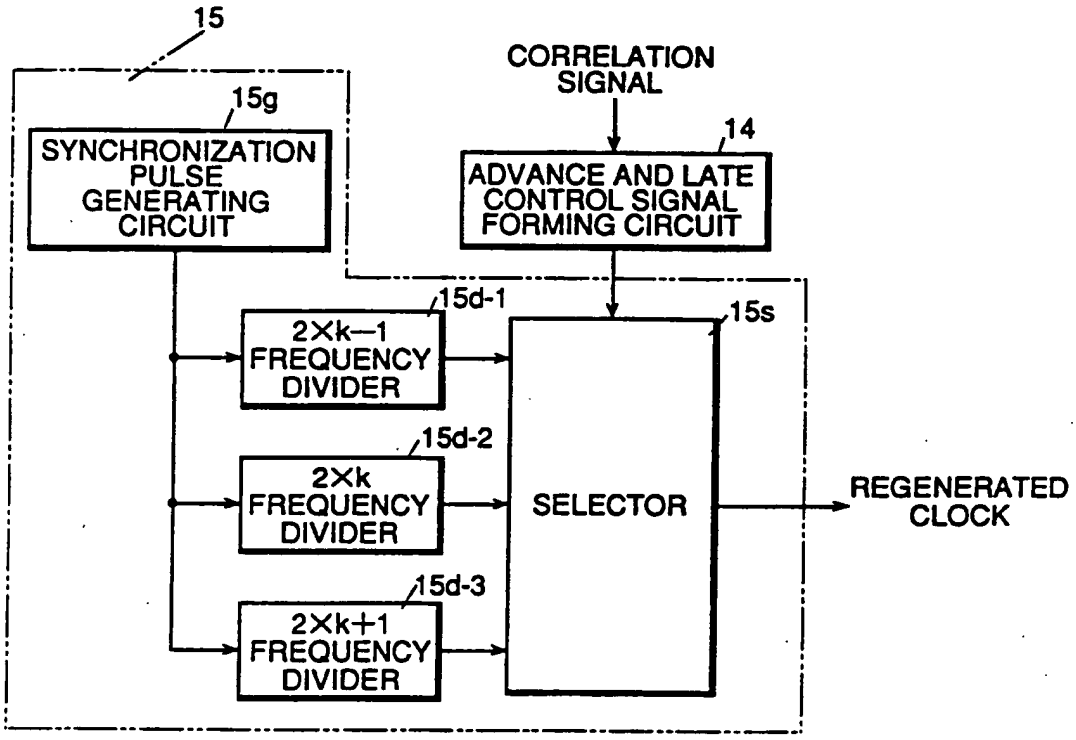

15
15g
SYNCHRONIZATION PULSE GENERATING CIRCUIT
CORRELATION SIGNAL
14
ADVANCE AND LATE CONTROL SIGNAL FORMING CIRCUIT
15d-1
2×k−1 FREQUENCY DIVIDER
15d-2
2×k FREQUENCY DIVIDER
15d-3
2×k+1 FREQUENCY DIVIDER
15s
SELECTOR
REGENERATED CLOCK

FIG.14

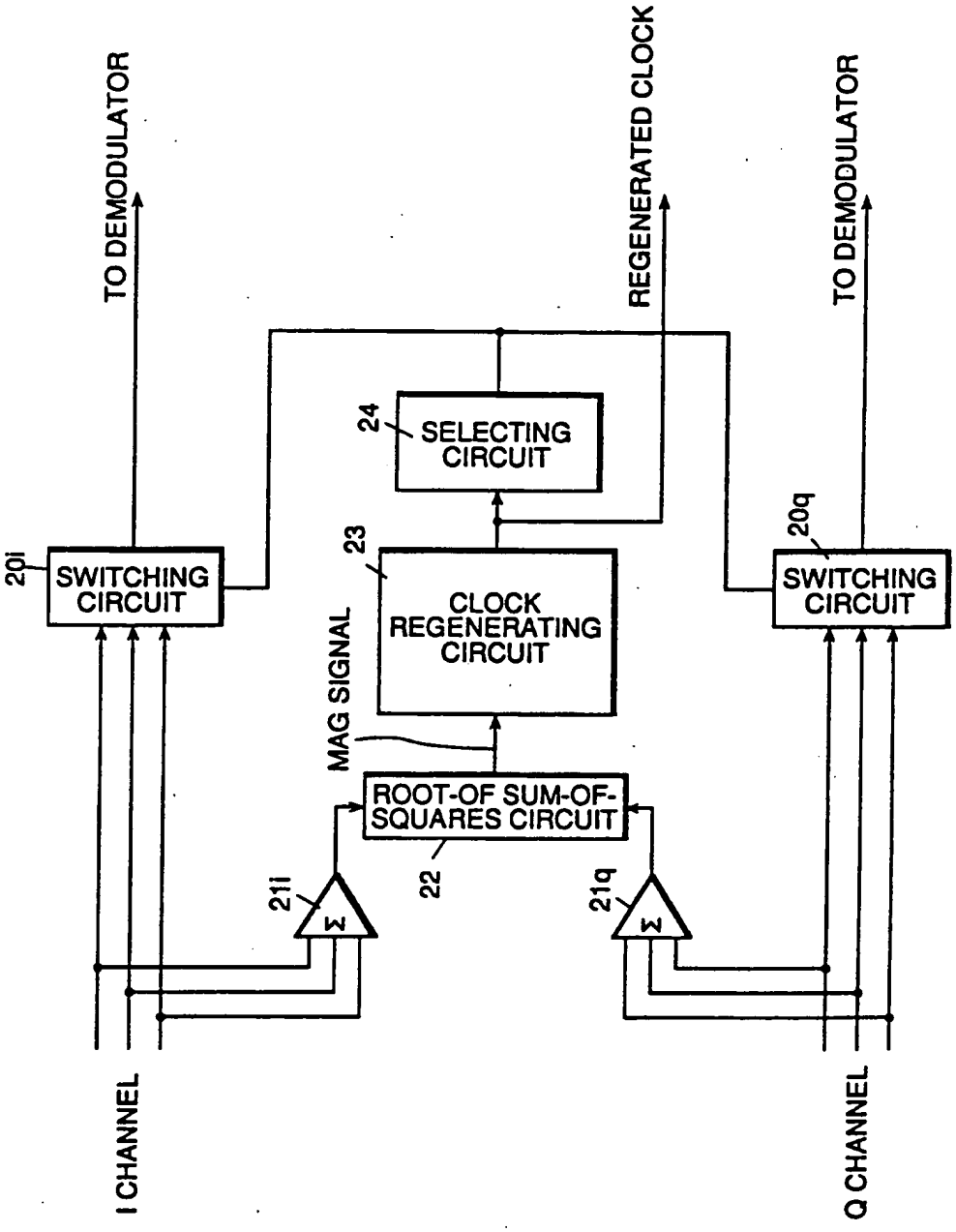

TO DEMODULATOR
REGENERATED CLOCK
TO DEMODULATOR
24
SELECTING CIRCUIT
20i
SWITCHING CIRCUIT
23
CLOCK REGENERATING CIRCUIT
20q
SWITCHING CIRCUIT
MAG SIGNAL
ROOT-OF SUM-OF-SQUARES CIRCUIT
22
21i
21q
Σ
Σ
I CHANNEL
Q CHANNEL

FIG.15

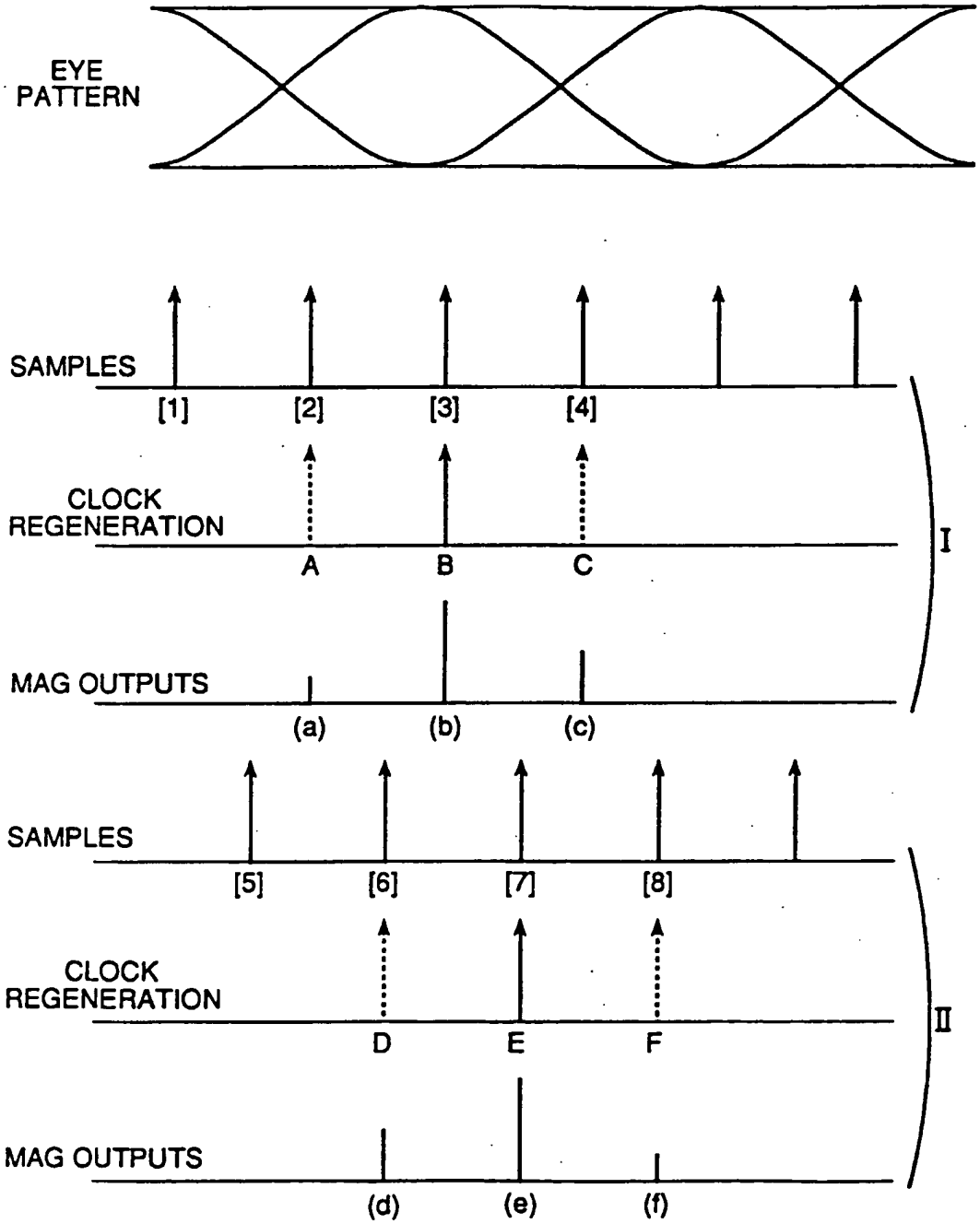

EYE PATTERN
SAMPLES
[1]
[2]
[3]
[4]
CLOCK REGENERATION
A
B
C
MAG OUTPUTS
(a)
(b)
(c)
I
SAMPLES
[5]
[6]
[7]
[8]
CLOCK REGENERATION
D
E
F
MAG OUTPUTS
(d)
(e)
(f)
II

FIG.16

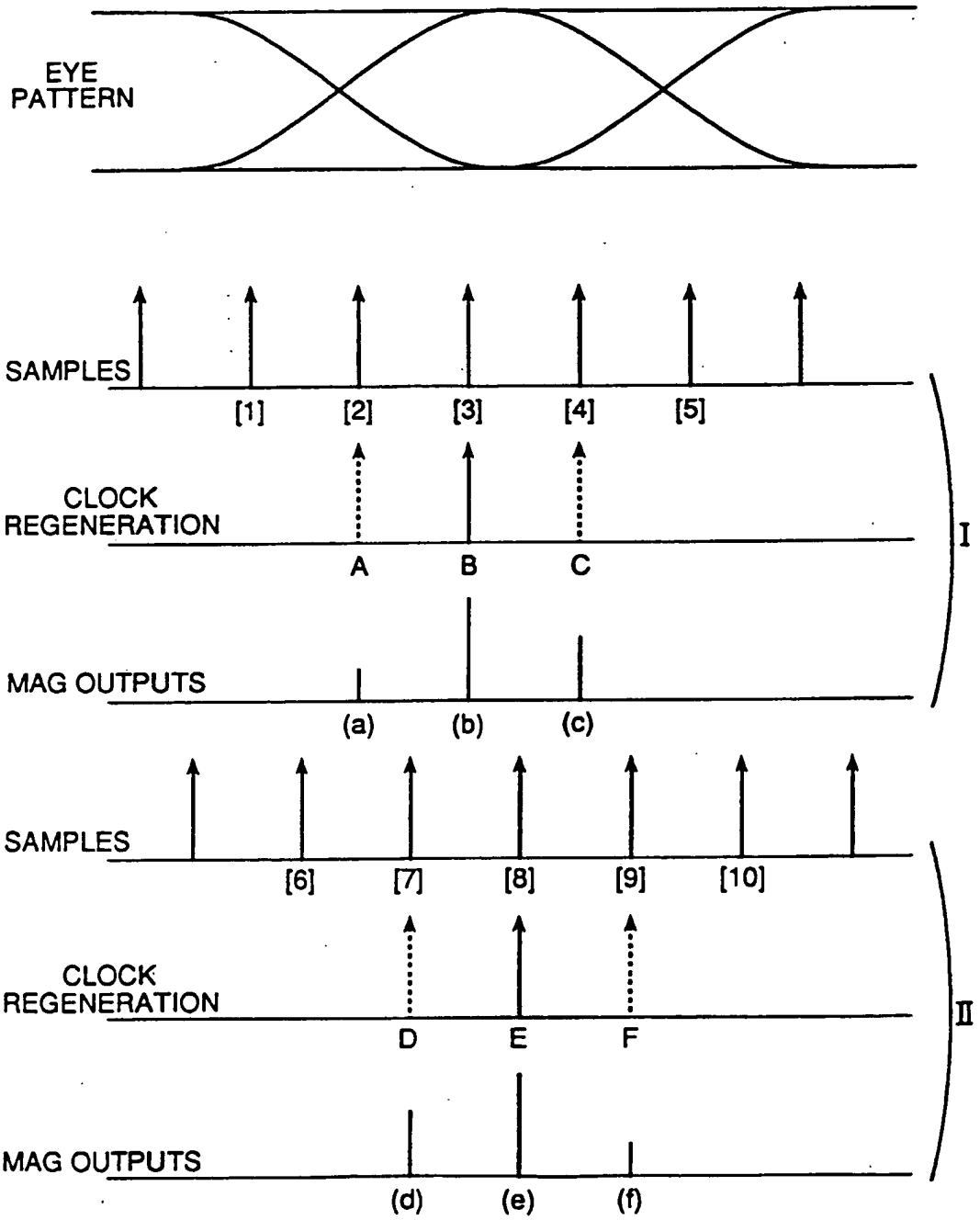

EYE
PATTERN
SAMPLES
[1]
[2]
[3]
[4]
[5]
CLOCK
REGENERATION
A
B
C
MAG OUTPUTS
(a)
(b)
(c)
I
SAMPLES
[6]
[7]
[8]
[9]
[10]
CLOCK
REGENERATION
D
E
F
MAG OUTPUTS
(d)
(e)
(f)
II

FIG.17

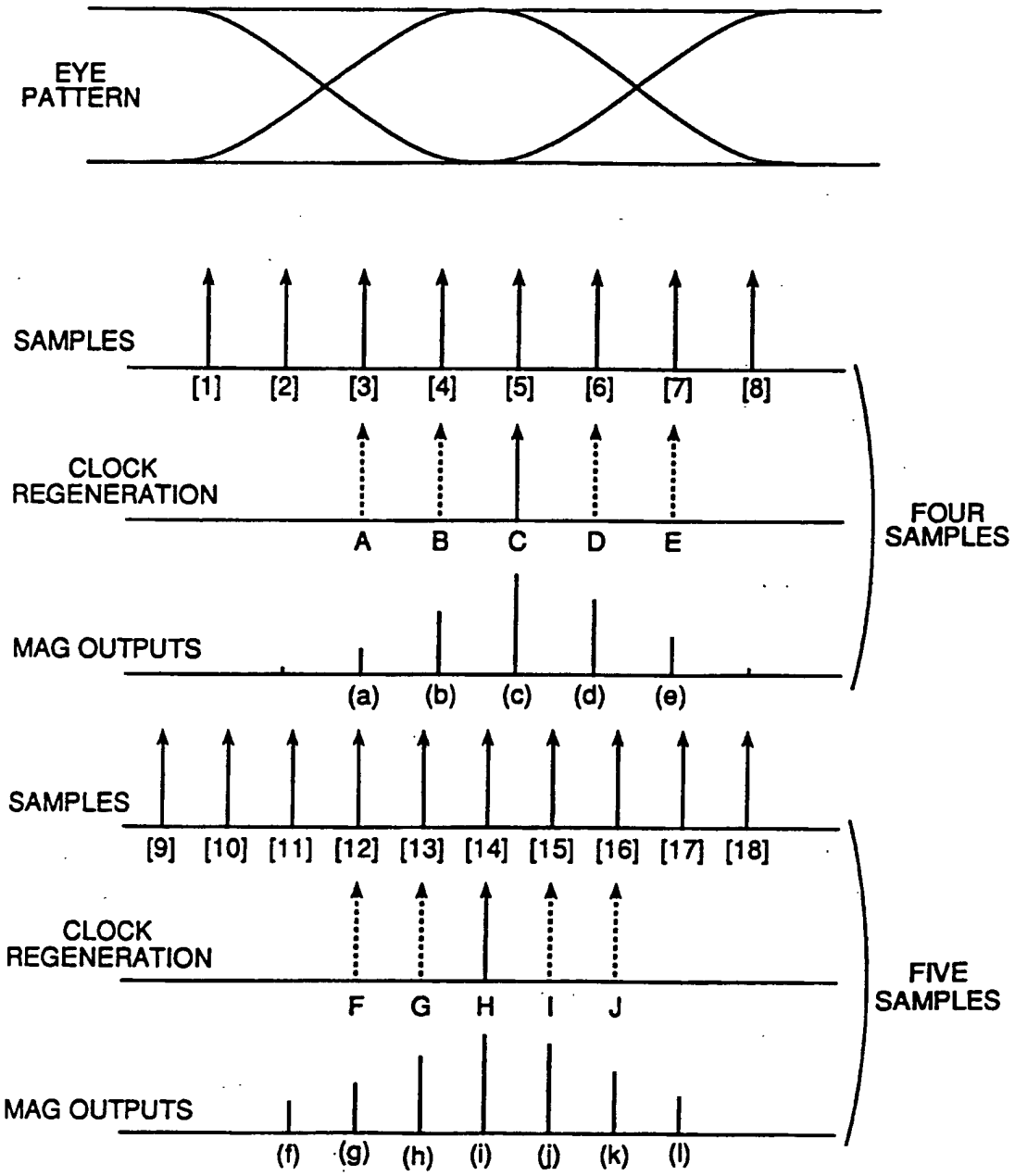

EYE PATTERN
SAMPLES
[1] [2] [3] [4] [5] [6] [7] [8]
CLOCK REGENERATION
A B C D E
MAG OUTPUTS
(a) (b) (c) (d) (e)
FOUR SAMPLES
SAMPLES
[9] [10] [11] [12] [13] [14] [15] [16] [17] [18]
CLOCK REGENERATION
F G H I J
MAG OUTPUTS
(f) (g) (h) (i) (j) (k) (l)
FIVE SAMPLES

FIG.18

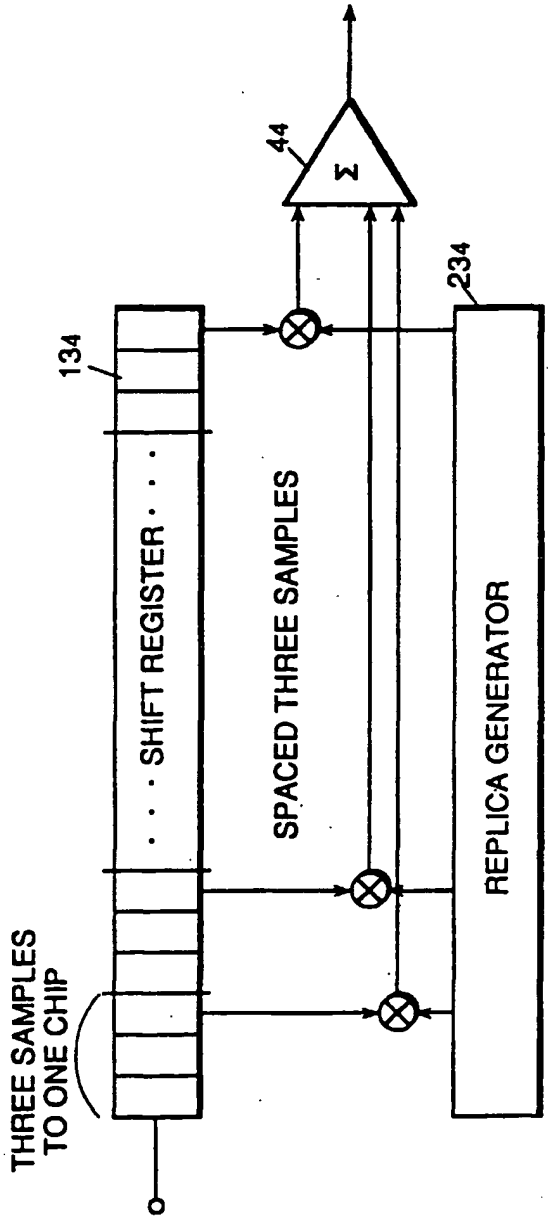

44
Σ
234
134
SHIFT REGISTER
SPACED THREE SAMPLES
REPLICA GENERATOR
THREE SAMPLES
TO ONE CHIP

FIG.19

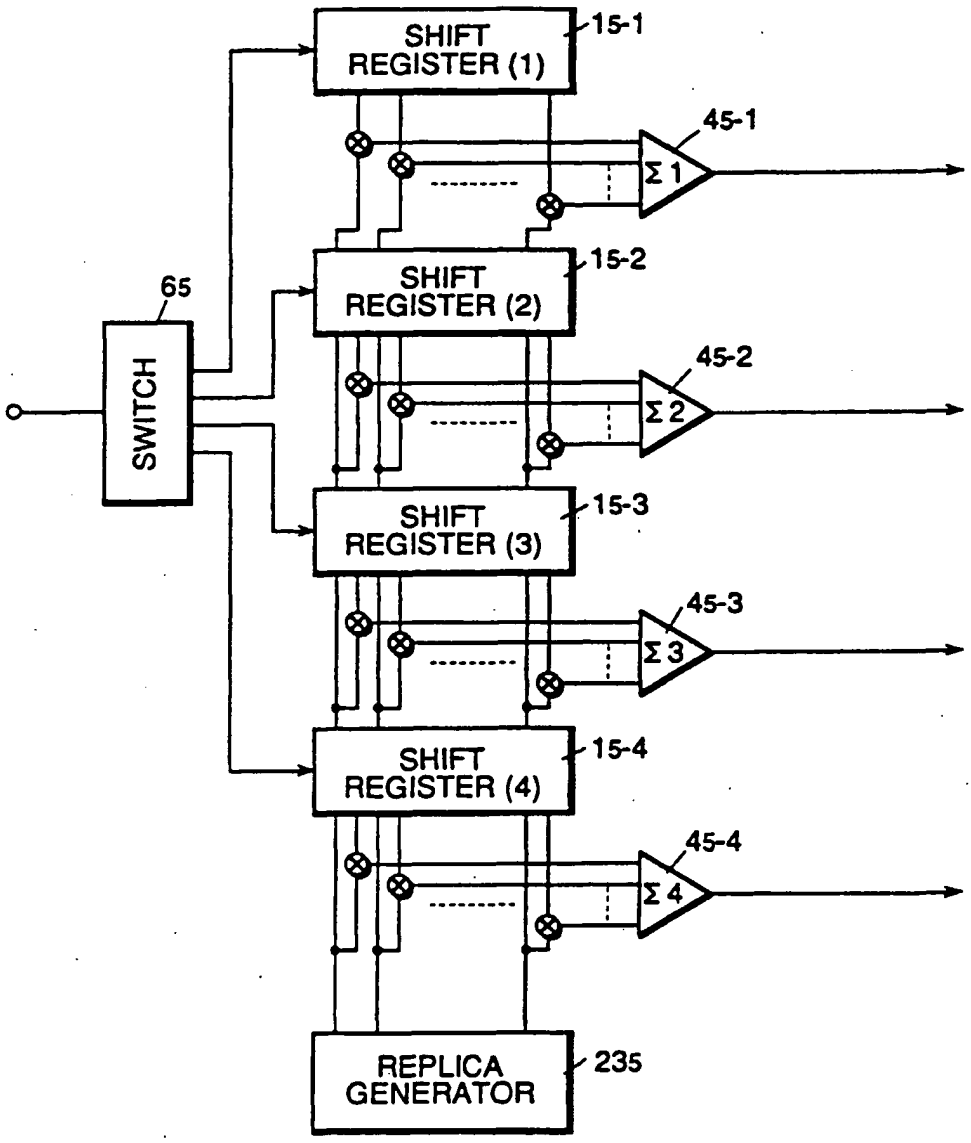

SHIFT REGISTER (1)
15-1
45-1
Σ 1
SHIFT REGISTER (2)
15-2
65
SWITCH
45-2
Σ 2
SHIFT REGISTER (3)
15-3
45-3
Σ 3
SHIFT REGISTER (4)
15-4
45-4
Σ 4
REPLICA GENERATOR
235

FIG.20

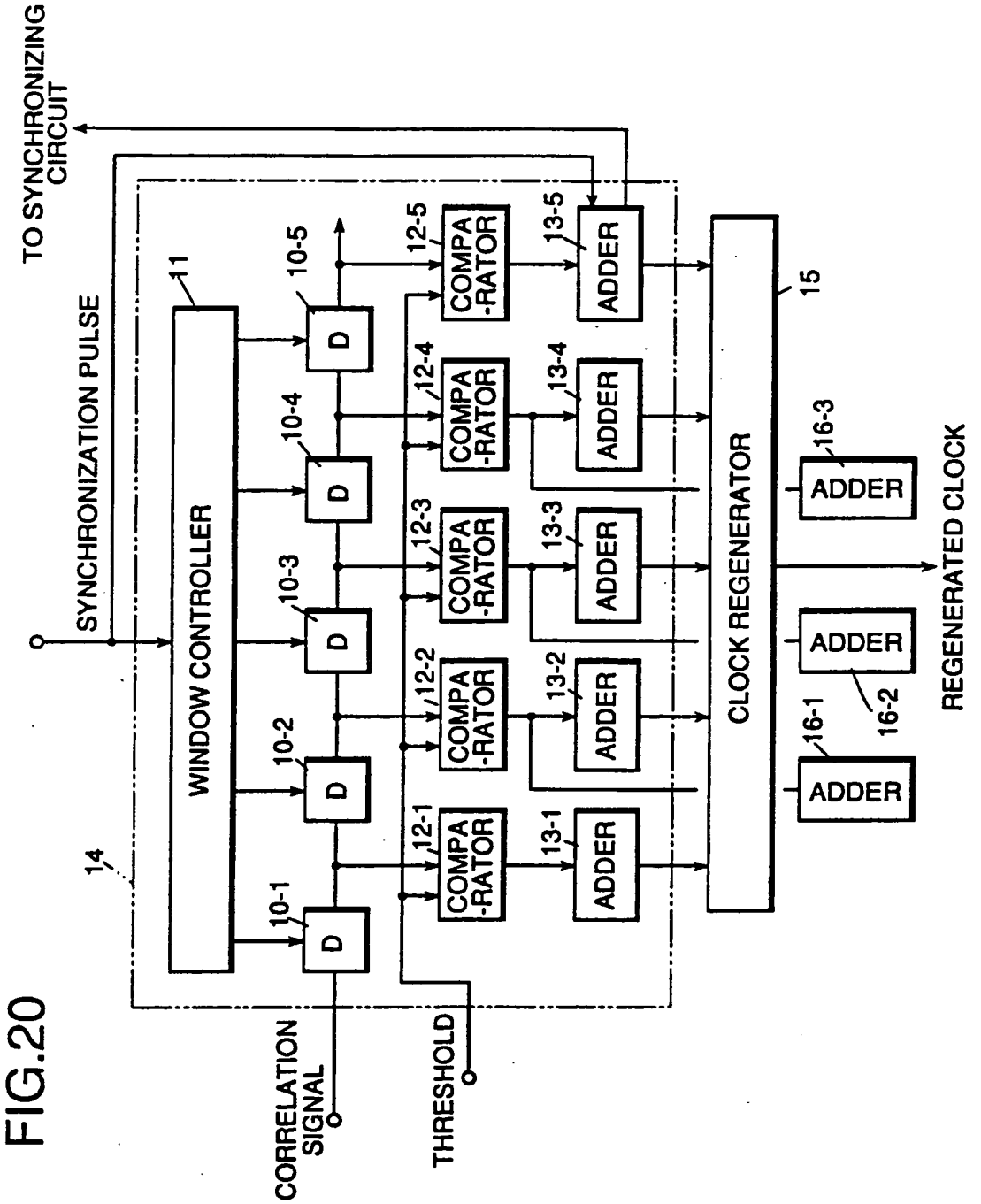

TO SYNCHRONIZING CIRCUIT
SYNCHRONIZATION PULSE
WINDOW CONTROLLER
11
14
D
10-1
10-2
10-3
10-4
10-5
COMPA-RATOR
12-1
12-2
12-3
12-4
12-5
ADDER
13-1
13-2
13-3
13-4
13-5
CLOCK REGENERATOR
15
16-1
16-2
16-3
CORRELATION SIGNAL
THRESHOLD
REGENERATED CLOCK

FIG.21

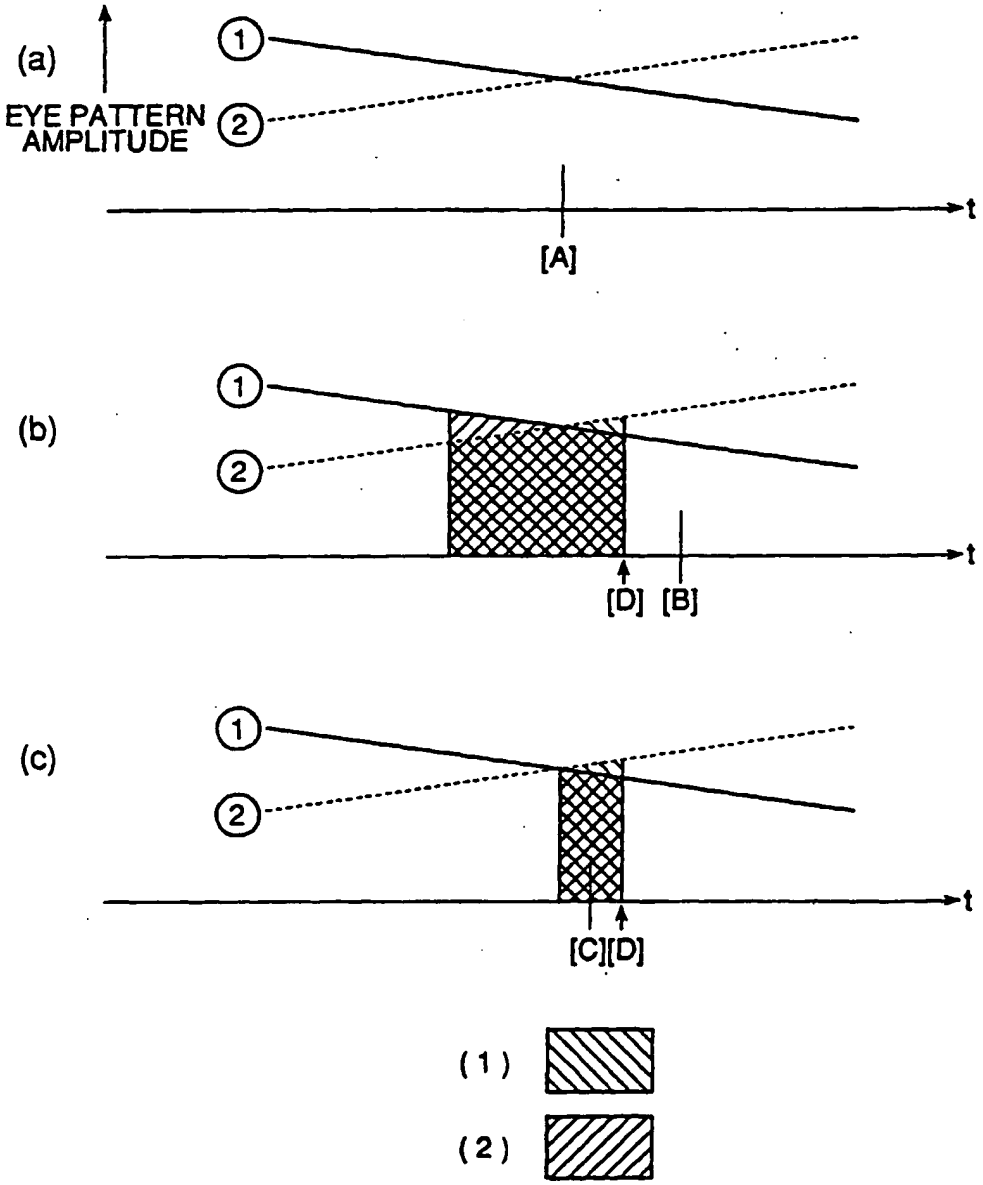
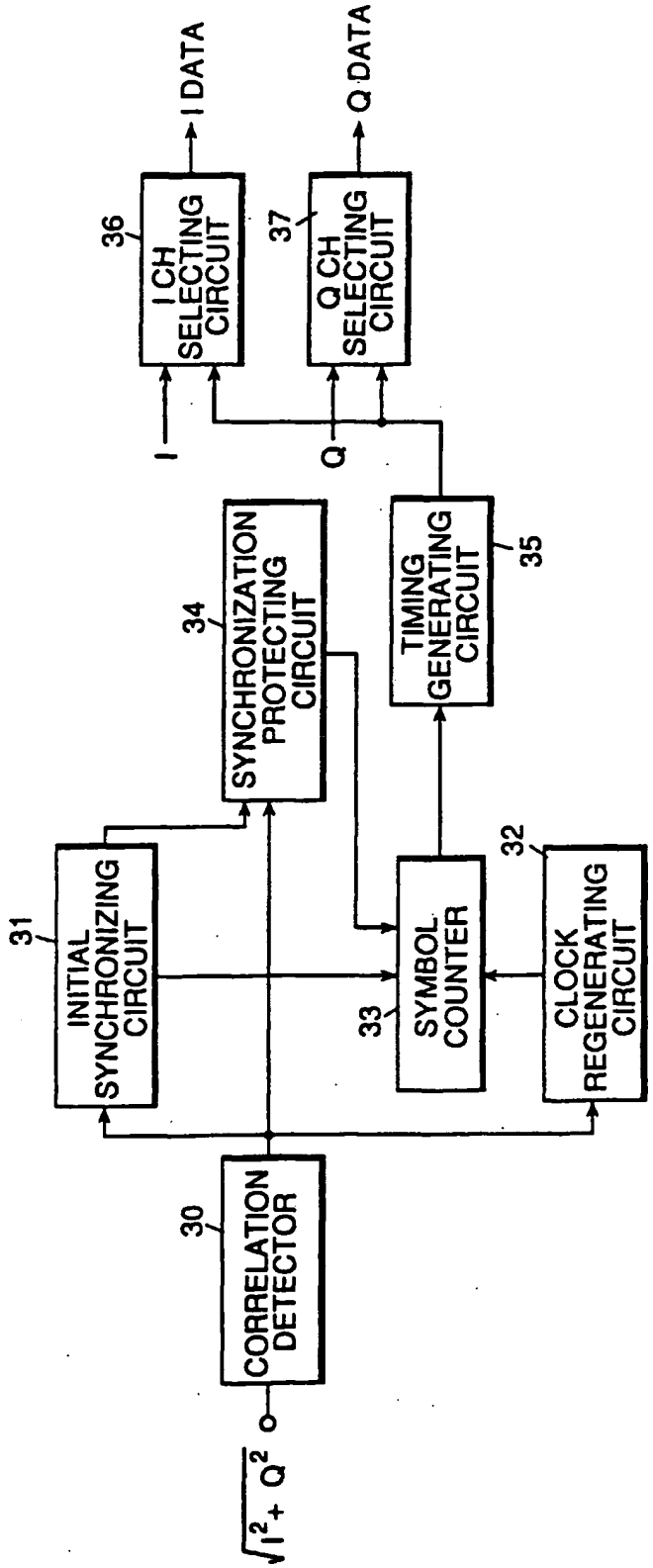


FIG.22


I DATA
Q DATA
36
I CH SELECTING CIRCUIT
37
Q CH SELECTING CIRCUIT
I
Q
34
SYNCHRONIZATION PROTECTING CIRCUIT
TIMING GENERATING CIRCUIT
35
31
INITIAL SYNCHRONIZING CIRCUIT
32
SYMBOL COUNTER
33
CLOCK REGENERATING CIRCUIT
30
CORRELATION DETECTOR
$\sqrt{I^2+Q^2}$